REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	June 27, 2002	Final Report for Period: Oct. 15, 1997- July 14, 2001

4. TITLE AND SUBTITLE
Device Quality, High Mis-Matched Semi conductor Materials Grown on si Substrates Using Unique Dislocation Engineering.

5. FUNDING NUMBERS
DAAG55-97-1-0111

6. AUTHOR(S)
Dr. Eugene A. Fitzgerald

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Mass. Institute of Technology
77 Massachusetts Avenue
Dept. of Electrical Engineering
Cambridge, MA 02139

(Sub-Contractor)
Prof. Steven Ringel
Ohio State University
2015 Neil Avenue
Columbus, OH 43210-1272

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U. S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
34763.13-MS

11. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.

12 a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

The ARO program focused on investigating and solving the basic materials science issues that historically have blocked the ability to achieve realistic, device-quality integration of III-V materials with Si. The level of understanding that we have achieved with respect to controlling the mismatched heteroepitaxy process has enabled breakthrough results in the materials science as well as the device technology aspects of this complex and promising heterostructure system. This final report reviews the approach used in this project, some of the important results we have achieved, and the applications now made possible. We finish the report with a list of publications, list of the students developed in this program, and pathways to commercialization for the basic technology developed in this program.

14. SUBJECT TERMS
Dislocation control, Lattice mismatch, Compositional graded buffer, Optoelectronic integration, GeSi, GaAs/Si, InGaP, Interdiffusion, Antiphase boundary,

15. NUMBER OF PAGES
40

16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION ON THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev.2-89)
Prescribed by ANSI Std. 239-18
298-102

1. Foreword

The ARO program focused on investigating and solving the basic materials science issues that historically have blocked the ability to achieve realistic, device-quality integration of III-V materials with Si. The level of understanding that we have achieved with respect to controlling the mismatched heteroepitaxy process has enabled breakthrough results in the materials science as well as the device technology aspects of this complex and promising heterostructure system. This final report reviews the approach used in this project, some of the important results we have achieved, and the applications now made possible. We finish the report with a list of publications, list of the students developed in this program, and pathways to commercialization for the basic technology developed in this program.

2. Table of Contents

3. List of Appendices, Illustrations, and Tables

List of Appendices

List of Figures

List of Tables

4. Statement of Problem and Research Approach

The research program was premised on developing a complete and correct understanding of how *material property* mismatch is introduced and can be controlled for heteroepitaxial systems that incorporate differences in lattice constant (*lattice mismatch*), crystal symmetry (polar/nonpolar), and chemistry (*heterovalency)*. Each type of dissimilarity introduces their own unique problems and working with a heterojunction system that combines all of these material differences may, in turn, lead to additional issues that could prove to be "show-stoppers" in their own right. Hence our program initially consisted of parallel efforts that independently focused on these issues. Once an understanding was developed to the extent that the problems associated with these independent types of dissimilarities were solved, the parallel efforts were merged in order to study and develop the entire III-V/Si system. UHVCVD was used to develop Ge/SiGe/Si layers, and both MBE (Molecular Beam Epitaxy) and MOCVD (Metal Organic Chemical Vapor Deposition) III-V growth methods were employed to integrate GaAs on Ge/SiGe/Si. MBE allowed us to take advantage of in-situ characterization to investigate basic growth and defect formation mechanisms, and we also were able to demonstrate the transfer of growth procedures to commercially-viable MOCVD that is prevalent in the commercial marketplace. As will be seen, the efficacy of the joint and complementary nature of our MIT-OSU program is born out by the major advances we have achieved during the course of this research. The next set of tables outlines the overall format of the program.

Phase I:

A. lattice constant engineering for highly-mismatched Ge on Si via graded SiGe buffers
- UHVCVD growth
- compositional grading from Si to Ge
- dislocations
- surface roughness

B. interface nucleation engineering for low mismatched, heterovalent GaAs on Ge
- MBE growth
- Interface cross-diffusion
- Anti-phase domains
- Surface roughness
- Minority carrier transport

A and B were conducted in parallel, at MIT and OSU, respectively

Phase II:

A. MBE growth studies of GaAs and AlGaAs/GaAs heterojunctions on Ge/GeSi/Si
- dislocations
- anti-phase domains
- interface cross-diffusion
- surface roughness
- minority carrier transport

B. MOCVD growth studies of GaAs on Ge and on Ge/GeSi/Si, MOVCD growth of InGaP graded layers on GaP
- dislocations
- anti-phase domains (GaAs/Ge/SiGe/Si only)
- surface roughness

A and B were conducted in parallel, at OSU and MIT, respectively.
Both A and B relied on MIT-generated graded GeSi buffers from Phase I.

Phase III:

A. Comparative studies of III-V growth on Ge vs. Ge/GeSi/Si
- anti-phase domains
- carrier lifetimes and minority carrier transport
- MBE and MOCVD approaches
- Non-stoichiometric (low temperature) III-V growth on Ge and Ge/GeSi/Si (AASERT to OSU) – not described here
- Graded InGaP structures on SiGe (AASERT to MIT) – not described here

B. Preliminary devices
- AlGaAs/GaAs diodes and photovoltaic cells on Ge and Ge/GeSi/Si
- InGaP/GaAs LED's and laser diodes on Ge/GeSi/Si
- Combined MBE/MOCVD grown InGaP/GaAs photovoltaic cells

A and B were conducted jointly at MIT and OSU.

Each phase led to the discovery of new science and also new problems, the latter of which were addressed as the program moved toward its final objective of generating basic AlGaAs/GaAs devices on Si via graded GeSi buffers. In all cases, there was significant collaboration, both at the PI level, and also at the student level, as the complementary skills at each institution were exploited to the maximum extent. Regular joint meetings were held between the MIT and OSU groups a few times per year, and close phone and electronic communication was continuous. The next several sections provide some highlights achieved by these efforts.

5. Summary of Most Important Results

5.1. Compositionally-Graded GeSi Buffers on Si: development of low defect density virtual substrates The initial MIT emphasis was to optimize the graded GeSi buffer growth using ultra-high vacuum chemical vapor deposition (UHVCVD). The optimization parameters were threading dislocation density (TDD), surface roughness and other gross surface features, since the purpose was to use the GeSi buffers to generate a Si wafer having the surface lattice constant of Ge, so that effective "low-mismatched" epitaxy of GaAs on Ge would be enabled. In other words, the generation of a "virtual Ge substrate" was the goal. The challenge was to achieve a low TDD value across large area (4 inch diameter) wafers so that these substrates would truly be of technological significance for III-V integration. Critical aspects of the UHVCVD growth process and compositional grading approach were identified and a growth parameter space that allowed us to achieve record low TDD for relaxed Ge on Si was developed.

We have previously shown that Ge graded layers on Si had lower threading dislocation densities than direct Ge growth on Si ($\rho \sim 10^7$ cm^{-2}).[1] However, this density is much too high for

minority carrier devices. Our understanding and modeling of the graded layer process revealed that the threading dislocation density should be constant with final Ge concentration for a constant grading rate (i.e. Ge%/μm). At that time, defect densities on the order of 10^6 cm^{-2} were being achieved for final Ge concentrations of 30% for 10% Ge/μm grading rates, yet 10^7 cm^{-2} were being achieved for final concentrations of 100%. We had traced the increased threading dislocation density with increased final Ge concentration to an interactive process between the surface morphology and threading dislocation flow.[2] The surface morphology resulted in the slowing of threading dislocations and trapping of threading dislocations into 'dislocation pile-ups', regions of dense threading dislocations lined up along wafer-plane <110> directions.

In this program, we sought to remedy this problem since high quality Ge and GaAs on Si was the goal. To this end, we conceived of an experiment to prove undeniably that the surface morphology was responsible for the threading dislocation density increase with increased final Ge concentration. The experiment was to stop grading growth at 50% Ge, create a uniform composition layer of a micron thickness, planarize that surface with a process like chemical-mechanical polishing to remove all surface morphology, and then re-insert that wafer into the CVD apparatus and regrow the rest of the graded layer to 100% Ge. As it turned out, this experiment not only proved that surface morphology/dislocation interaction was the mechanism responsible for the higher threading dislocation density, but the experimental procedure could also be used as a method for creating high-quality Ge on Si.[3]

Figure 1 is a schematic of the process on a microscale. Essentially, enough uniform thickness is grown on top of the graded layer as to allow the planarization to flatten the surface without polishing back into the graded region (polishing into the graded region results in the creation of many threading dislocations, since the surface cuts a plethora of misfit dislocations located in the graded region). Upon regrowth, the trapped threading dislocations are free to move once again, contributing to the strain relaxation process and obviating the need to nucleate more dislocations, which would increase the threading dislocation density.

Figure 2 shows the careful etch pitting (EPD) of surfaces of 50% Ge films and the regrowth on the 50% films after CMP. Note two striking features. First, the threading dislocation density is lower, overall, in the 100% Ge film than the 50% film. Second, note the decreased number of pile-ups (the dense threading dislocation areas) in the 100% Ge film. Upon accurate counting, we observe that the threading dislocation density and pile-up density actually improve with subsequent grading from 50% to 100%. This effect proves that the surface morphology is leading to the decreased threading dislocation mobility and concomitant increase in threading dislocation density. The effect also proves that dislocation annihilation plays an important role in graded composition layers. Calculations show that in grading from 50 to 100% Ge, there is not sufficient strain to push all of the missing threading dislocations to the edge of the wafer. Thus, the threading dislocations must be annihilated during flow. This conclusion led us to model the annihilation process, and we have determined that annihilation in these graded layers is very probable. Thus, a steady state view of the required number of threading dislocations which flow in a graded layer is valid, but we must remember that dislocation annihilation and nucleation are constantly occurring, leading to the steady state threading dislocation density that we observe in EPD experiments. Figure 3 shows that actually statistics of the wafers shown in Figure 2. Note that both field threading dislocation densities (i.e.

threading dislocations away from the pile-ups) and the pile-up threading dislocation densities (the density in the pile-up regions) decrease after the planarization process and subsequent grading to 100%. Also note that a CMP process at 25% improves the defect density in 50% Ge wafers.

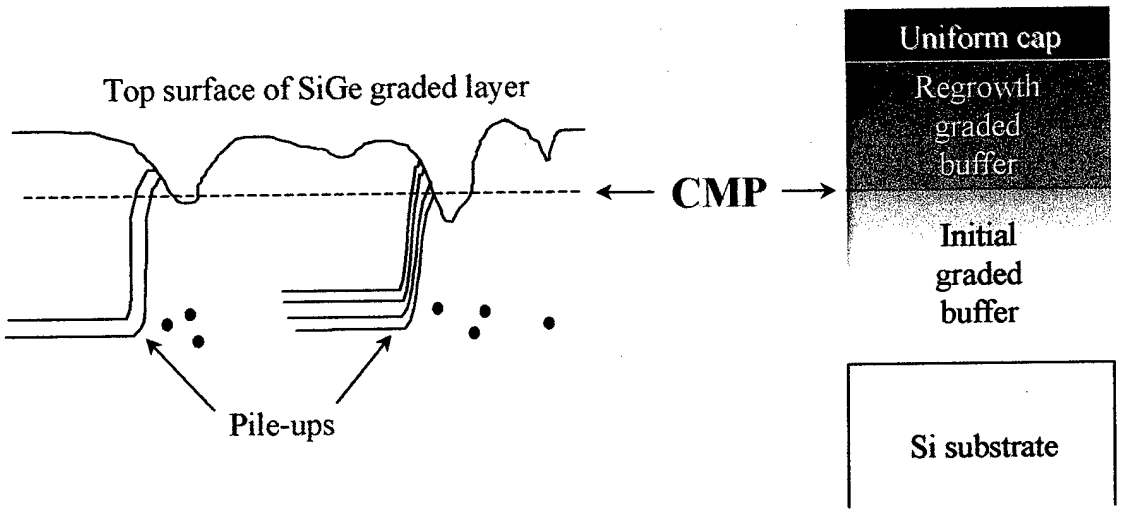


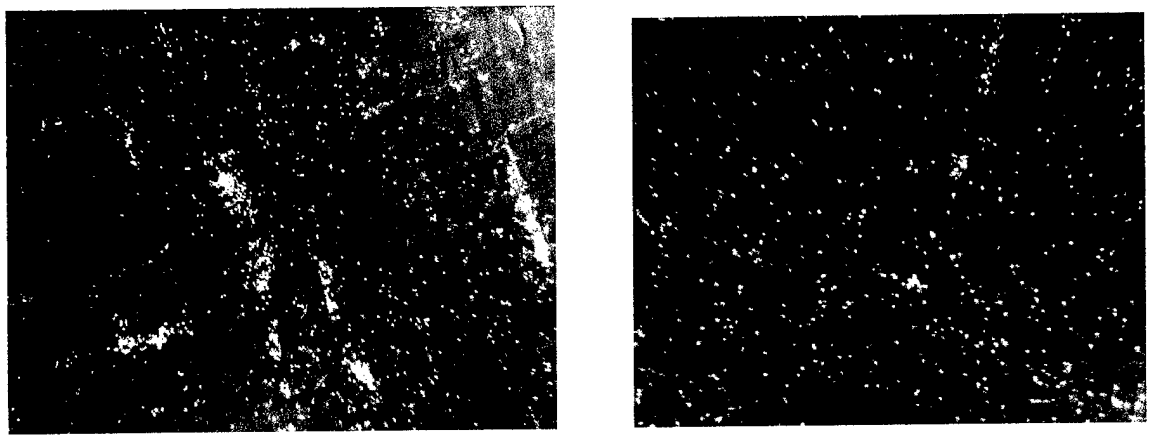
Figure 1: Schematic showing the procedure for un-pinning the threading dislocations at a dislocation pile-up. A uniform composition layer is grown such that the surface can be planarized without penetrating the graded layer which contains many misfit dislocations.

During the program, other improvements in the handling of wafers, control of particles in the loading environment, etc. have also led to a decrease in threading dislocation densities, although the CMP process is the largest factor in improving threading dislocation density at high Ge concentrations. Figure 4 is a plot of our current best threading dislocation density measurements. The data for all compositions represent improvements of at least one order of magnitude improvement since the beginning of the ARO program. To plot this reduction success, Figure 5 is a plot of threading dislocation densities in relaxed SiGe versus time.

Finally, we mention our ability to control the strain state of Ge at room temperature, despite a large thermal expansion difference between Ge and Si. The lattice mismatch between Ge and Si is compressive, i.e. Ge has a larger lattice constant than Si. Thus, SiGe alloys grown on Si substrates that are not completely relaxed possess in-plane lattice constants that are smaller than their relaxed constants, creating biaxial compression. However, in bringing a Ge/Si structure to room temperature from growth temperature, the difference in thermal expansion coefficient between Ge and Si results in tensile Ge at room temperature if the Ge were relaxed at growth temperature. Thus, a problem with completely relaxed Ge on Si is that much tensile strain can be present at room temperature; in fact enough to create cracks in the Ge layer.

We have shown in this program that we can purposely retain unrelieved compressive lattice-mismatch in the pure Ge on SiGe/Si at the growth temperature, and thereby compensate for the tensile thermal expansion stress that is introduced on cooling the wafer from growth

temperature. X-ray diffraction results show that the Ge can be cubic at room temperature (i.e. unstrained) following this procedure.



(a) (b)

Figure 2: (a) EPD of 50% Ge alloy surface; (b) and EPD of a regrowth on (a) after CMP of (a), grading to a final composition of Ge at the surface in (b). Note the few pile-ups that remain after CMP and regrowth, and detailed counting shows that the overall threading dislocation density is decreased as well.

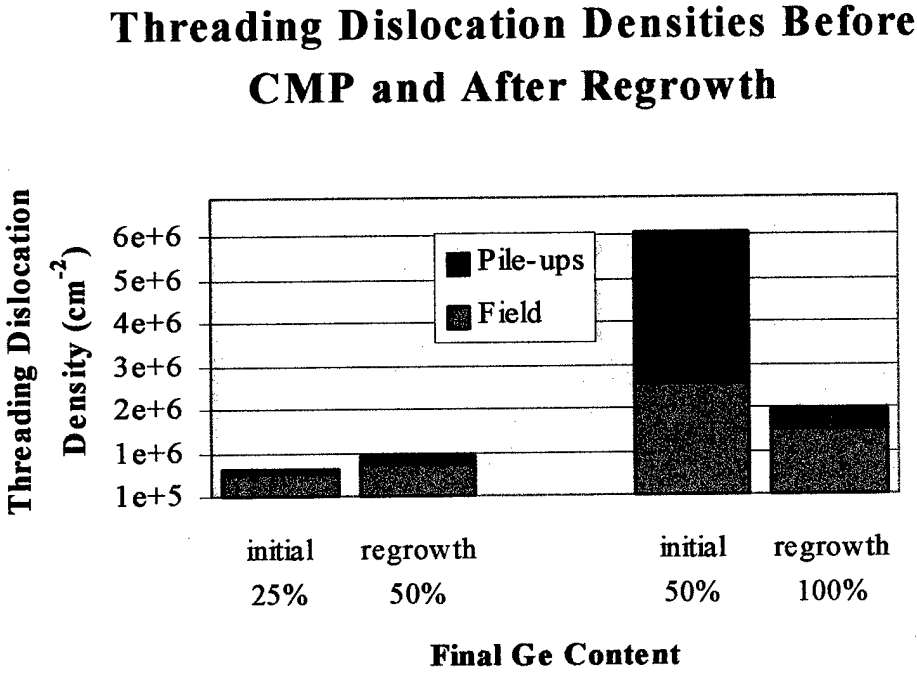


Figure 3: Statistics from the 50% and 100% wafers shown in Figure 2, as well as statistics from 25% Ge graded layers, and 25% layers with CMP and regrowth to 50% Ge layers. Note that in all cases, the CMP step lowers pile-up density and threading dislocation density

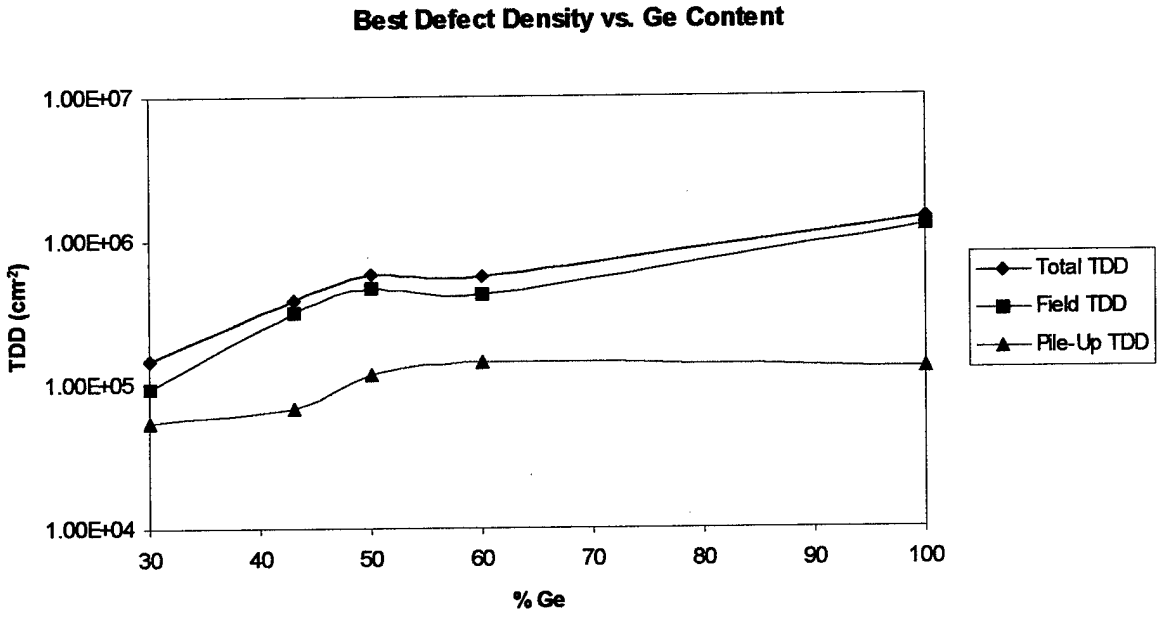


Figure 4: Best threading dislocation densities in relaxed SiGe alloys for a variety of final Ge concentrations in the film. All layers are graded to final composition using approximately 10% Ge/μm grading rates.

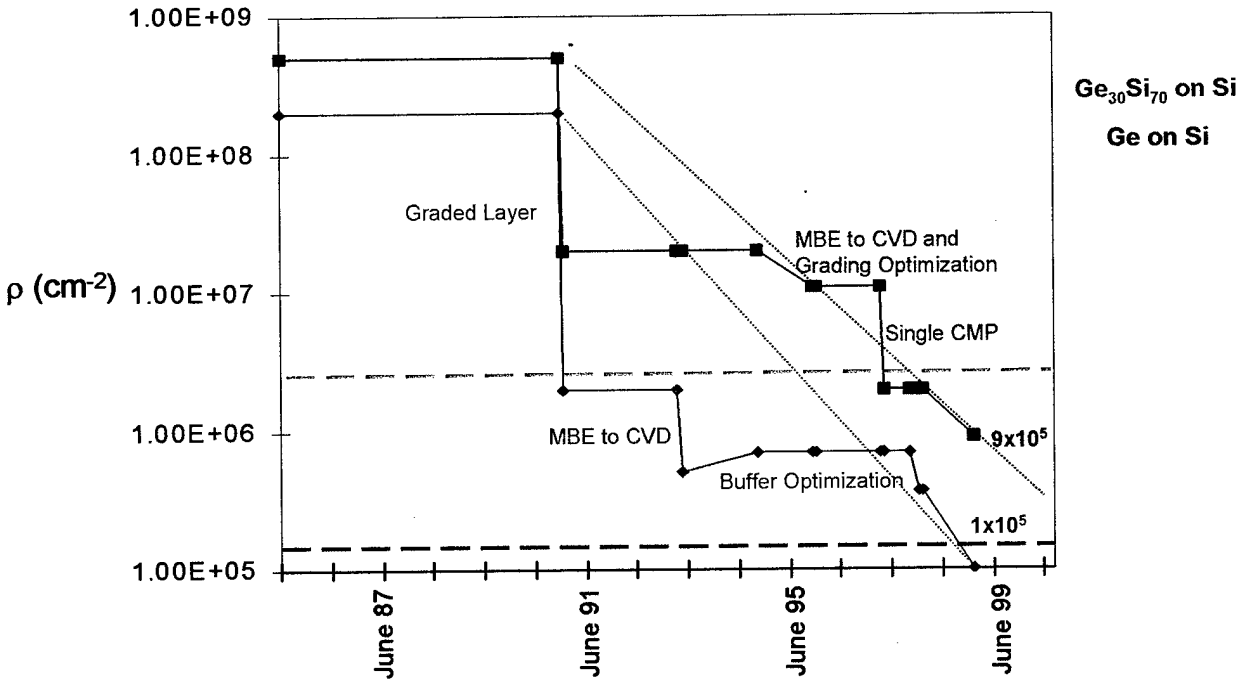


Figure 5: Improvement in threading dislocation density in relaxed 30% Ge alloys on Si and relaxed pure Ge on Si. The green line symbolizes the threading dislocation density below which minority carrier devices can perform well, and the red line symbolizes the theoretical limit for growth temperatures near 900C.

5.2. Graded buffer modeling. The CMP process revealed much new information about the nature of threading dislocation motion, annihilation, and trapping in graded relaxed SiGe layers. This information improved our understanding of graded buffer relaxation, and therefore stimulated us to improve our mathematic expressions for modeling, and encouraged us to look for similarities in other materials systems. First, in order to aid others in using our results, we re-formulated our previous dislocation flow model in terms of practical variables,[4]

$$\rho_t = \frac{2R_g R_{gr} e^{\frac{U}{kT}}}{bBY^m \varepsilon_{eff}^m} \qquad (1)$$

where R_g is the growth rate, R_{gr} is the grading rate, U is the activation energy for dislocation glide, T is the temperature, b is the Burgers vector, B is an elastic constant, Y is the Young's modulus, and ε_{eff} is the effective strain. In addition, we embedded the concept with this formula that if experiment shows a higher threading dislocation density than expected, that the effective strain must be decreasing, which means that some mechanism is slowing down or blocking threading dislocation motion. In the case of SiGe, this surface morphology is the mechanism.

In 5.6, we will describe the results from the InGaP/GaP graded layer system. We seeded investigations in this materials system to extend our understanding of grading in all systems in the context of Equation 1. Also, this system has the practical utility of creating visible light emitting diodes (LEDs) with transparent substrates, leading to high efficiency LEDs through improved light extraction. In the case of InGaP/GaP, the methodology embedded in Equation 1 led us to conclude that in this case, unlike the SiGe case, new two-dimensional defects were responsible for interacting with threading dislocations and slowing their velocity during growth.

5.3. GaAs heteroepitaxy on Ge: interfaces, defects, and growth optimization of a low-mismatched, heterovalent heterostructure The initial OSU emphasis was to investigate and optimize the formation of an *ideal, low-mismatched GaAs/Ge interface* in parallel with the optimization of the GeSi buffer development, in anticipation of transferring this knowledge to III-V growth on Ge/GeSi/Si substrates. In this way we first could assess our ability to characterize and suppress antiphase domains (APD's) and cross diffusion prior to introducing the complications associated with the GeSi buffer, such as surface crosshatch, higher residual TDD, and the potential presence of thermal strain. Along this vein, GaAs epitaxial layers and AlGaAs/GaAs DH structures were grown by MBE on offcut (001) Ge wafers. We experimented with a range of GaAs nucleation conditions – As versus Ga stabilized Ge surfaces, As_2 versus As_4 nucleation, migration enhanced epitaxy (MEE), growth temperature, in-situ annealing, etc, as well as including a thin, < 20 nm, epitaxial Ge layer atop the Ge wafer. Using a combination of in-situ RHEED measurements made in real-time video with post-growth TEM, SEM, EBIC and AFM studies, we were able to determine a set of growth conditions that reproducibly yielded GaAs layers with no evidence of APD disorder, even to a monolayer scale.[5]

For MBE growth, we identified both the thin Ge epitaxial layer and an in-situ anneal in excess of 600 C as necessary to completely eliminate APD disorder, even at the interface-scale, for growth on (001) Ge substrates that were offcut by 6° toward the <111> direction. RHEED showed that the anneal was necessary to recover the desired double-atomic step height surfaces from the offcut substrates, but that APD-free films were still not possible until we included a thin, Ge epitaxial layer on the Ge wafers prior to GaAs nucleation. Subsequent Auger and SIMS studies revealed the Ge epitaxial layer acts to suppress carbon surface segregation and clustering from the Ge substrate wafer during the oxide desorption and annealing steps prior to growth, which otherwise acts as nucleation sites for disordered growth.[6]

After Ge epitaxy, GaAs growth was initiated using migration enhanced epitaxy (MEE) deposition step at 350 C of GaAs for 10 monolayers, prior to conventional MBE growth. APD-free GaAs layers were achieved using either As and Ga initiation, substantiating theoretical claims that this should be possible. We found that initiating the MEE step with either Ga or As_2 yielded the same (2x4) surface domain for GaAs, suggesting that an energetically favorable surface domain is present for (001) GaAs grown by MBE on Ge. Interestingly, we did observe a complete 90-degree rotation of the surface domain to (4x2) by RHEED, but only when using As_4 initiation, while still maintaining APD-free material. The mechanism for this difference is not understood at present.

Once high structural quality growth was reproducibly achieved, we began to simplify our growth conditions to anticipate the move to the Ge/GeSi/Si substrates. We found that APD-free GaAs could also be achieved without the initial MEE step, by simply initiating the usual co-evaporation of Ga and As but at a reduced substrate temperature of 500 C for several hundred nm prior to conventional growth at 620 C. RHEED showed that this co-evaporation method for initiation rapidly produced a single domain surface, suggesting that a surface re-ordering phenomenon was thermodynamically preferred at these growth conditions. Extensive APD disorder was observed only when the Ge epitaxial buffer was not grown on the Ge wafer and/or when the substrate received an incomplete pre-growth anneal to generate the double-stepped surface structure emanating from the substrate offcut angle. For these cases, RHEED showed a mixed 2x4:4x2 surface reconstruction that closely correlated with ex-situ, post-growth TEM results which showed extensive APD disorder. As stated above, this led us to conclude that clusters of carbon contaminants from the original Ge wafers were likely sources for APD formation, even for vicinal surfaces (a point which may explain the difficulty in APD suppression for many users of "vendor Ge substrate wafers"). Figure 6 shows typical RHEED images taken after several monolayers of GaAs epitaxy for growth initiation conditions that lead to APD formation and APD suppression. Figure 7 summarizes the impact of controlled growth initiation conditions on long range APD formation. Note that by proper nucleation, APD formation is completely eliminated, even at the monolayer scale. As will be evident in subsequent paragraphs, this is crucial for the practical development of III-V devices on Si since the elimination of III-V buffer layer thickness is critical to lessen the thermal expansion mismatch strain that is generated between the III-V layers and the underlying Si wafer.

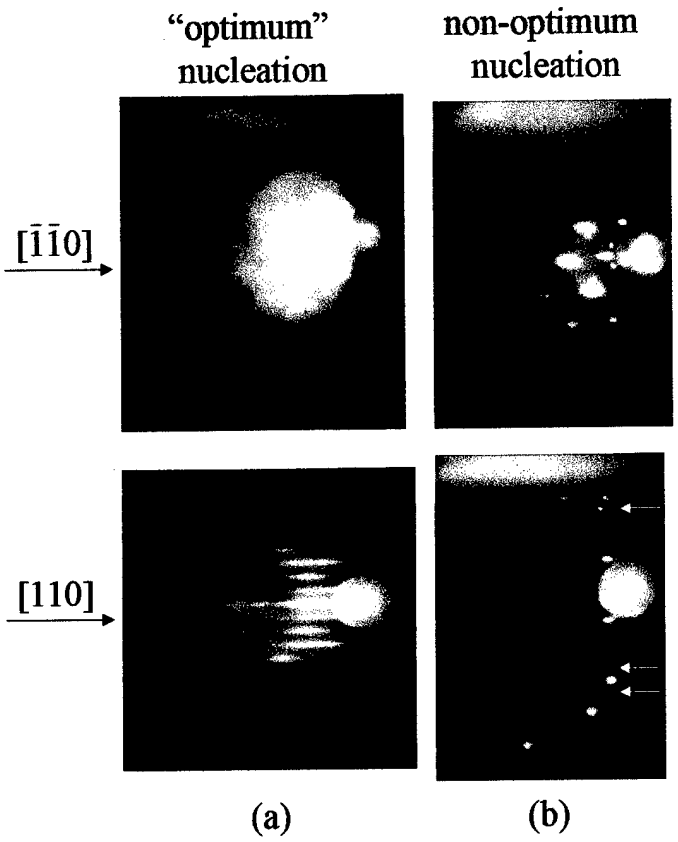


Figure 6. (a) RHEED image after several monolayers of GaAs growth on offcut (001) Ge showing (a) optimal and (b) non-optimal patterns for orthogonally incident e-beam conditions. The 4th order diffraction spots indicated by the arrows in (b) result from the presence of 2x4 and 4x2 surface structure, indicating mixed domain growth and APD formation. The blurry pattern for one direction of (a) is due to interference by the double stepped surface.

A final, but very important result from this phase of the research program was the near-complete suppression of atomic cross diffusion at the GaAs/Ge interface. In anticipation of having to deal with the large mismatch in thermal expansion between the GaAs/Ge layers and the Si substrate wafer, it is necessary to eliminate or minimize the presence of inactive GaAs

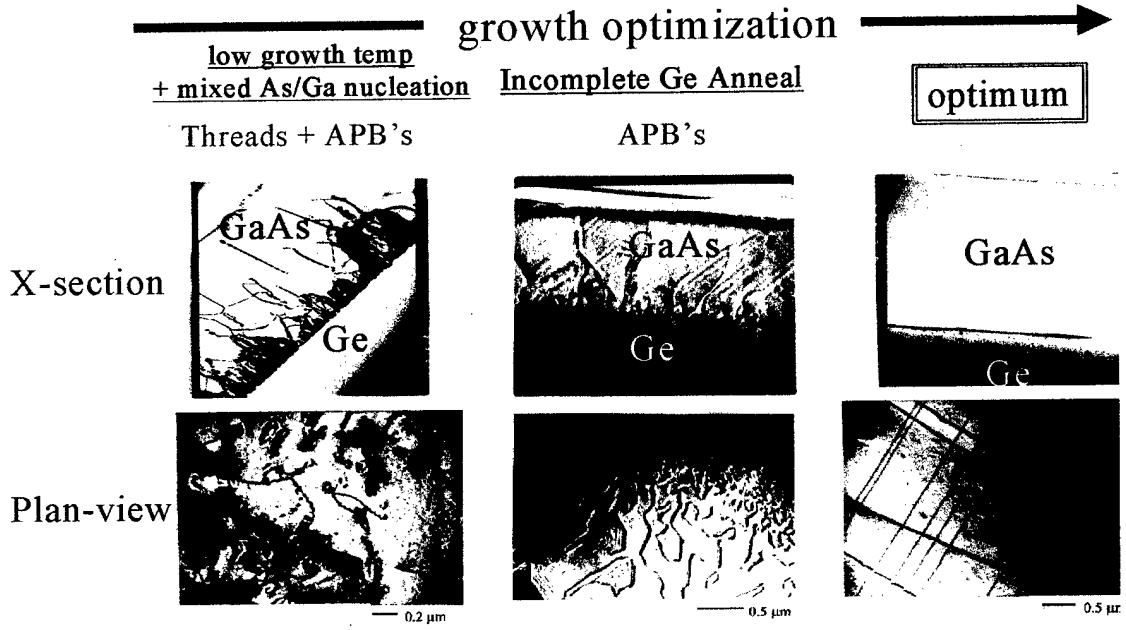


Figure 7. Cross section and plan view TEM images of MBE grown GaAs on offcut (001) Ge wafers indicating the types of defect morphologies present and the success of our optimal nucleation conditions to eliminate APD formation and rampant threading dislocation formation. The optimal conditions lead to an array of misfit dislocations as shown, with TDD below TEM statistical detection, consistent with an ideal, low mismatched interface.

buffer layers that other groups have found necessary to "bury" autodoping effects below active layers. Extremely thick layers will contribute to wafer bow and potential cracking (an issue for proposed investigation in this proposal). Extensive SIMS and C-V doping profile data indicates that the MBE growth process we have developed maintains any Ge "outdiffusion" into the overlying GaAs layer to less than $2x10^{15}$ cm^{-3} within 0.1 um from the GaAs/Ge interface, yields no detectable (below SIMS limit) Ga "in-diffusion" and limits As "in-diffusion" to less than $1x10^{18}$ cm^{-3} within the first ~ 0.5 microns of the underlying Ge substrate.[7] Moreover, in constrast to the APD results, the MEE nucleation was important in that it minimizes the amount of As "in-diffusion," which we tentatively attribute to inhibiting surface exchange reactions at the heterovalent interface. These results are shown in the next section, alongside a similar study for GaAs growth on the Ge/GeSi/Si substrates, where this finding has the most impact.

5.4. GaAs and AlGaAs/GaAs heteroepitaxy on defect-engineered Ge/GeSi/Si substrates by MBE

Subsequent to completing the work described in section 5.3, we immediately began investigating the behavior of our GaAs/Ge growth scheme on the Ge/GeSi/Si substrates developed by the initial phase of the MIT effort. Since the higher surface roughness introduced by the crosshatch of these substrates made RHEED evaluation of APD formation ineffectual, we relied on post-growth structural and electrical studies to investigate the transfer of our GaAs/Ge growth methodology to these "virtual Ge" substrates. Figure 8 shows a cross sectional TEM micrograph of an AlGaAs/GaAs/AlGaAs double heterostructure (DH) used for subsequent time resolved photoluminescence (TRPL) lifetime studies. At this scale, no threading dislocations are evident, similar to our TEM results within the relaxed Ge terminating layer of the graded buffer.[8] Additionally, there is no evidence of APD disorder, even at fine TEM scales. To more fairly assess the quality of these heterostructures, lower magnification EBIC and EPD studies were initiated, from which we counted threading dislocation densities from $7x10^5$ cm^{-2} to $2x10^6$ cm^{-2} for samples over a wide range of Ge/GeSi/Si substrate growth conditions. In all cases, the TDD values in the GaAs overlayers closely matched the TDD values in the final Ge layer of the graded buffer. This demonstrates from the structural perspective that we have successfully maintained an "ideal, low-mismatched" GaAs/Ge interface on Ge/GeSi/Si substrate wafers.

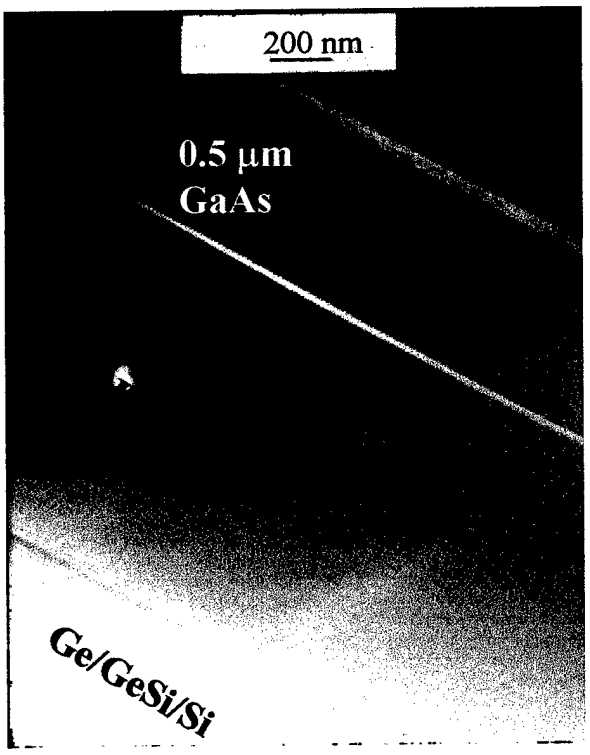


Figure 8. Cross sectional TEM image of MBE grown AlGaAs/GaAs DH structure indicating that an ideal, low mismatched GaAs/Ge interface has been achieved on graded GeSi/Si buffers.

As mentioned above, cross-diffusion is a very important issue for generating III-V devices on Si. Figure 9 summarizes the cross-diffusion results from the MBE GaAs growth on both Ge and Ge/GeSi/Si substrates.[9] Clearly, cross-diffusion of As, Ga and Ge is virtually negligible, indicating that III-V buffers used to separate device layers from highly autodoped regions is not necessary. In fact, although not shown, C-V doping results on GaAs that were intentionally doped to $1x10^{15}$ cm^{-3}, showed no increase in concentration to within 0.5 microns of the GaAs/Ge interface, demonstrating that III-V devices which require very low doping concentrations should be feasible.

It is important to note here that Ge 'out-diffusion' during vapor phase growth is not a bulk atomic diffusion process. In fact, we have confirmed our speculation that severe auto-doping in this system is due to atom surface exchange during growth, i.e. that Ge tends to exchange with Ga and As atoms that are depositing on the surface, causing a Ge 'tail' to extend

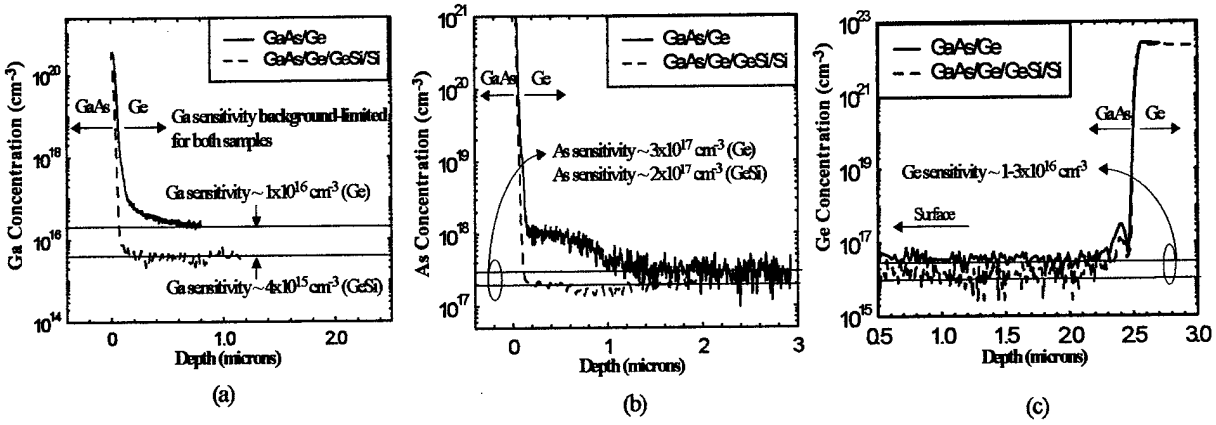


Figure 9. SIMS data indicating minimal interdiffusion at the GaAs/Ge interface of a) Ge, b)As, and c)Ga for both the Ge wafer and the Ge/GeSi/Si graded buffer under similar interface initiation conditions.

into the GaAs crystal. For the temperatures and times in which this phenomena occurs, we can clearly see that bulk diffusion would lead to much less interdiffusion than what is observed. Thus, the Ge presence in GaAs is an entirely kinetic one, and can be influenced greatly by the growth conditions. In MBE growth, by initiating growth at moderate or low temperatures, we can suppress surface exchange. Once 2-3 monolayers of GaAs are deposited, the surface exchange mechanism is no longer possible, which is why raising growth temperature to a higher more optimal temperature at this point does not create massive interdiffusion. Therefore, the process of initiating growth at low temperature is valuable since it eliminates the surface exchange mechanism, forcing bulk diffusion to be the only operative mechanism for interdiffusion.

Since the ultimate application of these mismatched heterostructures are optoelectronic and electronic devices, we began extensive studies of the electronic properties of these heterostructures on Ge/GeSi/Si. The minority carrier lifetime is an excellent and very sensitive indicator of "device-quality" material. Hence, a large number of AlGaAs/GaAs/AlGaAs DH structures were grown in order to determine the dependence of carrier lifetime, measured by TRPL decay, on III-V growth conditions, substrate growth conditions, and on the presence of varying TDD and APD disorder. Investigations on both Ge and Ge/GeSi/Si substrates were made. The results are summarized by the data in Table 1. As seen, both high lifetimes and low AlGaAs/GaAs interface recombination velocities were achieved on a consistent basis. In fact, prior to this work, the highest reported minority carrier lifetime for GaAs grown on Si was in the

2-3 nanosecond range. *Our work has increased this by a factor of 4-5*, achieving room temperature lifetimes in excess of 10 nanoseconds for n-GaAs doped at $1x10^{17}$ cm^{-3}.[10] Note that this factor of 4-5 is extremely important, since this factor pushes the lifetime across a critical

Table I: Compilation of lifetime data for 29 DH samples with similar growth conditions ($n=1x10^{17}$ cm^{-3}). GaAs buffer thickness indicates the proximity of the GaAs DH to the GaAs/Ge interface. In all cases, APD formation was suppressed.

Sample	Substrate	GaAs buffer thickness (μm)	S (cm/s) (T=300 K)	τ_p (ns) (T= 300K)
A-C	Ge#	0.1	$9 x10^3$	19.0
D-F	Ge	0.1	$2.9 x10^3$	19.4
G-I	Ge	0.5	$2.8 x10^3$	17.2
J-L	Ge/GeSi/Si	1.0	$3.9 x10^3$	7.7
M-O	Ge/GeSi/Si	0.5	$1.3 x10^3$	6.6
P-R	Ge/GeSi/Si	0.1	$2.2 x10^3$	8.3
S-U	Ge/GeSi/Si	0.1	$1.9 x10^3$	6.4
V-X	Ge/GeSi/Si	0.1	$1.9 x10^3$	6.8
Y	Ge/GeSi/Si	0.1	$2 x10^3$ *	9.4
Z	Ge/GeSi/Si	0.1	$2 x10^3$ *	10.5
AA	Ge/GeSi/Si	0.1	$2 x10^3$ *	8.6
BB	Ge/GeSi/Si	0.1	$2 x10^3$ *	8.5
CC	Ge/GeSi/Si	0.1	$2 x10^3$ *	7.9

#Indicates substrates without UV-Ozone treatment.

*Indicates samples where multiple data points were not available. For these cases, τ_p was calculated assuming S = $2x10^3$ cm/s.

barrier at 1-2ns. A plot of minority carrier device performance vs. minority carrier lifetime will show that a sharp discontinuity in GaAs device performance occurs at the 1-10ns range. Thus, 1ns and shorter tends to result in poor device performance, and approximately 10ns and longer results in good minority carrier device performance. As long as APD's were suppressed in the structure (the presence of which caused very low lifetimes and high interface recombination velocities), we found the lifetime to systematically track the TDD value, as shown in Figure 10. Here, the measured lifetimes are plotted along with theoretical predictions of lifetime vs. TDD values at this doping concentration for GaAs.[11] This comparison is significant from a few perspectives. First, we can conclude that residual threading dislocations are the dominant lifetime-killers in these materials, confirming that no lifetime-killing defects result from the GaAs epitaxy onto Ge/GeSi/Si and the only major defects are the residual threading dislocations from the upper part of the GeSi graded buffer, as hoped. Second, the lifetime and TDD values are very close to the knee of the plateau, below which additional increases in carrier lifetime due to continued reduction in TDD will be slight (at this doping concentration). Third, a lifetime value of 10 nanoseconds is already high enough to support the fabrication of high performance minority carrier devices (of course, majority carrier devices are much less sensitive to carrier lifetime so this is an even less stringent situation). Last, but most certainly not least is the fact that we have achieved this record-high quality material for GaAs DH structures using a GaAs buffer layer having a thickness of just 0.1 microns (see table 1). We did not observe any degradation of electronic quality as the buffer was thinned from 1 micron down to this value,

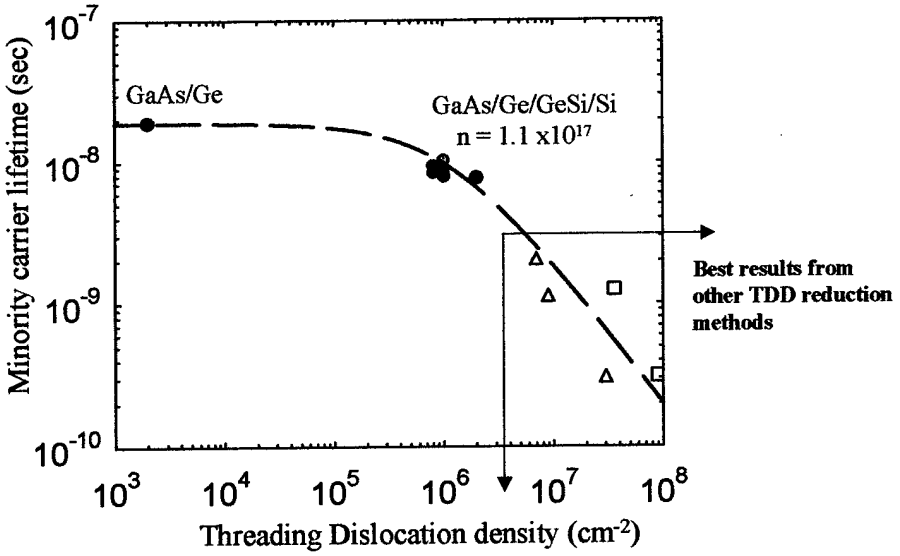


Figure 10. Plot of minority carrier lifetime versus threading dislocation density. The dashed line plots the theoretical dependence calculated found from ref. 11 assuming τ_{po} = 19ns (τ_{po} determined from GaAs/Ge control samples on a Ge substrate). The GaAs/Ge/GeSi/Si lifetimes are the highest reported for GaAs/Si. The good agreement with theory indicates that the residual TDD's emanating from the GeSi buffer limit the lifetime in our samples and confirm that the GaAs/Ge interfaces in these high mismatched structures behave as ideal low mismatched interfaces.

demonstrating the complete encapsulation of severe mismatch defects below the GaAs/Ge interface.

Taking the structural and electronic material quality data together, this body of work clearly demonstrates that device-quality III-V materials can be generated via a combination of optimal GeSi compositional grading with careful nucleation of the GaAs/Ge interface. This was the major goal of program. The next section discusses our progress in transferring this knowledge to the MOCVD growth environment, and also the new level of understanding achieved for MOCVD III-V growth onto Ge/GeSi/Si substrates. This section is followed by a summary of the preliminary device results we have achieved.

5.5. GaAs and AlGaAs/GaAs heteroepitaxy onto defect-engineered Ge/GeSi/Si substrates by MOCVD Growth of GaAs on Ge using MOCVD is known to be problematic.[12] The approach taken in this research was to use the MBE, with the in-situ diagnostics, as the tool to analyze the ideal surface conditions, and then translate this knowledge to MOCVD.

During our study of MOCVD GaAs growth on Ge/SiGe/Si, we observed that the quality of the material can be influenced by many factors, including substrate off-cut, low levels of residual As in the atmospheric MOCVD tool, temperature of growth initiation, and even cooling rate of Ge from high to low temperature just before GaAs growth initiation. The results are too numerous to list in detail here, but the reader can be referred to the MIT thesis of Dr. Steven

Ting, and his publications listed in this document. Here, we summarize the overall accomplishment of high quality GaAs growth on Ge/SiGe/Si using MOCVD.

Figure 11 shows typical GaAs grown on Ge/SiGe/Si if one follows typical growth conditions for GaAs in MOCVD. Since the GaAs/Ge system is a nearly lattice-matched system, it is incredible that the defect morphology in this system can be as bad as GaAs grown directly on Si. Numerous antiphase boundaries are present at the interface, which can block the motion of threading dislocations that are necessary to relieve the small amount of lattice-mismatch between GaAs and Ge. Thus, the heterovalency of the interface turns a very small lattice mismatch into a severe defect problem. In fact, a range of defect morphologies can be created in MOCVD using different temperatures for first exposure to As.

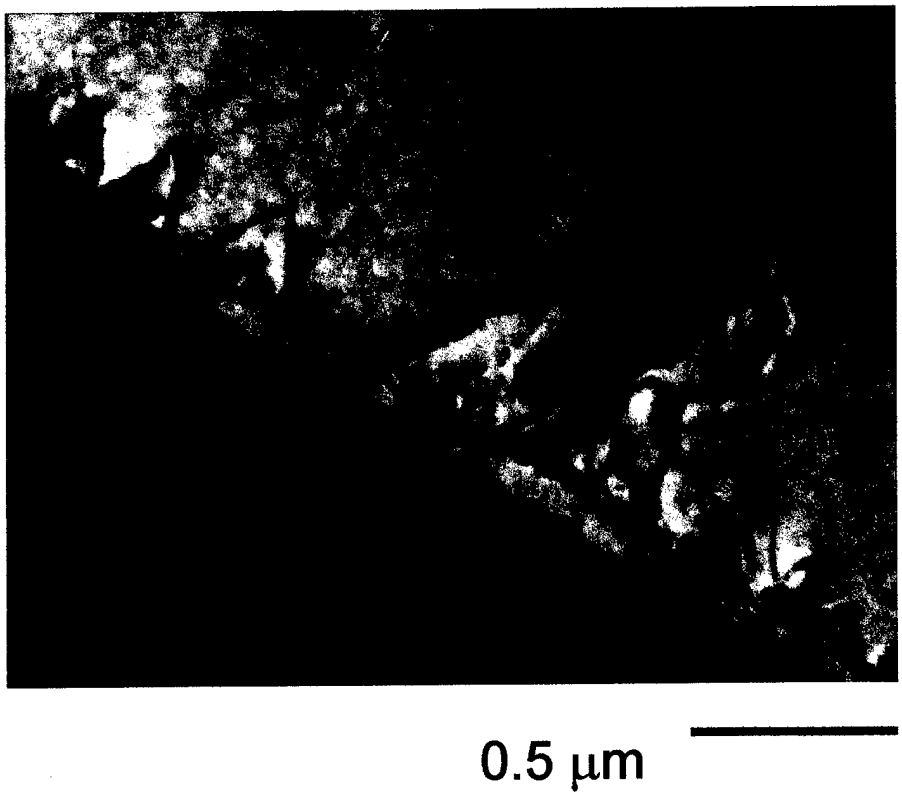


Figure 11: Cross-section TEM micrograph of GaAs on Ge/SiGe/Si using MOCVD and standard growth conditions. Note the triangular shaped anti-phase boundaries, which are very deleterious to high quality growth. Threading dislocation motion is hampered by the anti-phase boundaries, leading to high threading dislocation densities even though the lattice mismatch between GaAs and Ge is small.

A key observation that we observed in our MOCVD reactor is the time transient in cooling the wafer from desorption temperature to first GaAs growth. Summarizing the MOCVD procedure that is necessary for high quality GaAs/Ge growth, we first heat the wafer to 650C for 15 minutes, then cool to the desired nucleation temperature, usually 400-500C. Initiation with arsine flow at this temperature is performed, followed by turning on the trimethyl gallium flow to start GaAs growth. After a few tens on nm's, the temperature can be raised to the optimum GaAs growth temperature, in our reactor ~650C.

In cooling down from >650C to the low temperature initiation point, we have conclusively shown that different APD morphologies on the GaAs wafer can be achieved. Single domain films can be produced, but slow cooling must be performed to achieve this, especially through the 450-600C temperature window. For a full atomic-level interpretation of these results, see reference 13.

Once we had discovered the intricacies of the MOCVD GaAs/Ge growth, we were able to produce high quality (low threading density, no APDs) GaAs on Ge using MOCVD, as shown in Figure 12. Excellent diodes have been fabricated from this material (Figure 13).

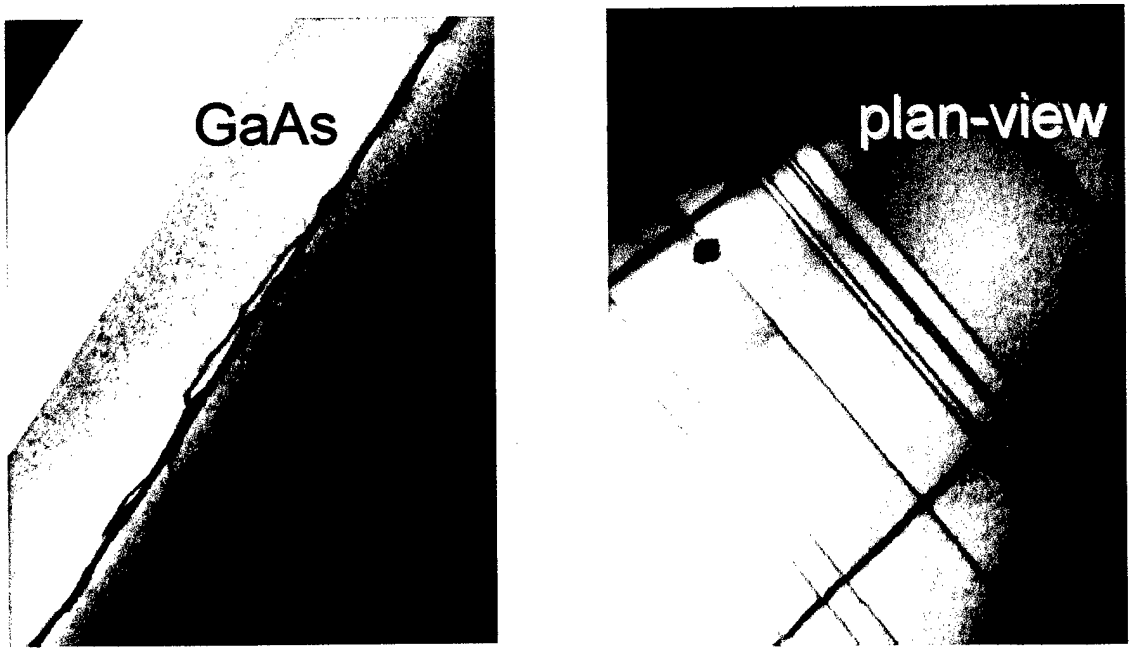


Figure 12: Cross-section and plan-view TEM micrographs of GaAs/Ge/SiGe/Si layers grown via MOCVD (only GaAs/Ge interface shown). Note the lack of threading dislocations in the images, the well-behaved orthogonal array of misfit dislocations, and the lack of anti-phase boundaries at and above the interface.

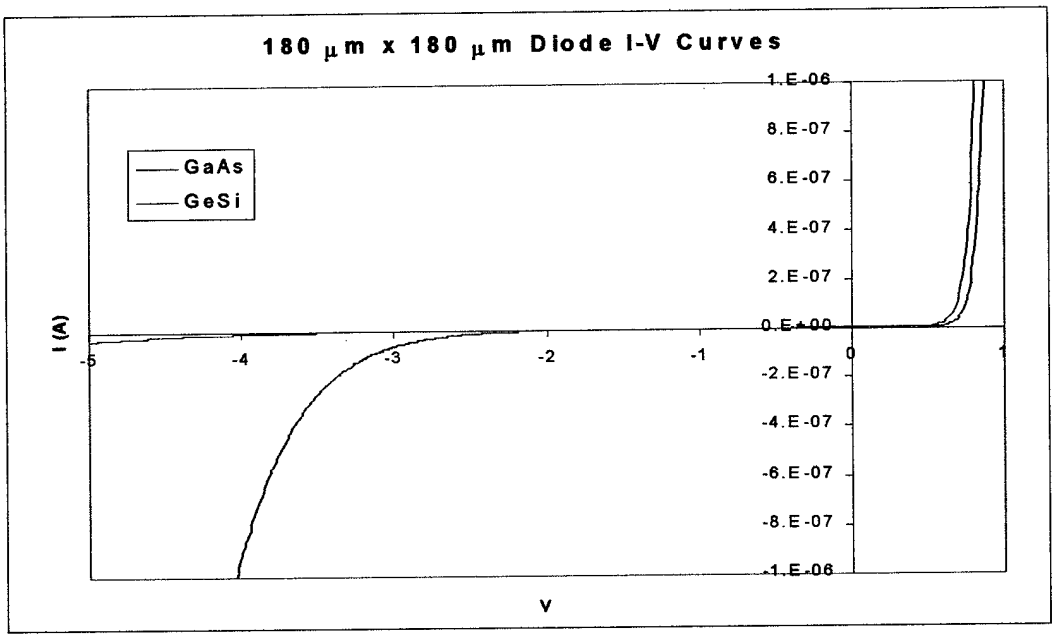


Figure 13: I-V plots of GaAs diodes grown by MOCVD on Ge/SiGe/Si. Note the excellent I-V characteristics and the good reverse breakdown. These diodes were early indicators that the material quality was nearing the quality needed for minority carrier devices. The legend refers to GaAs diodes on GaAs substrates, and GaAs diodes on Ge/SiGe/Si substrates.

5.6. InGaP graded layers on GaP substrates As mentioned previously in the buffer modeling section, we decided to investigate other materials systems for applicability of our model and graded buffer methodology. InGaP/GaP is an interesting system since as one adds In to GaP, the indirect band gap remains and has the same value, but the lattice constant changes from that of GaP to InGaP at about 50% In, which is lattice-matched to GaAs. At about 30% In, InGaP becomes direct and the band gap decreases with further In concentration increases. If graded layers of InGaP are used to accommodate lattice constant differences between InGaP layers and GaP substrates, the material in the graded layer and the GaP substrate are transparent to the wavelength of the InGaP final layer. Thus, if an LED were to be fabricated from the InGaP layer (say at a composition of In corresponding to an emission of yellow, orange, or red), the substrate and all other layers would be transparent, and maximum external power efficiency can be obtained, since no absorption is occurring.

Despite these commercial advantages, InGaP graded layers on GaP have not been successful. Early work showed that quantum efficiency decreased as grading continued,[14] suggesting a rise in threading dislocation density as InGaP layers are graded to higher In

compositions. We decided to use our modeling from the SiGe/Si graded system to explore the InGaP/GaP graded system.

Figure 14 shows that indeed, that our first InGaP graded layers on GaP resulted in a rising threading dislocation density as further grading is done. As nature would have it, when the alloy compositions with the direct band gap are achieved in a graded structure, the threading dislocation densities are too high to be useful materials in LEDs. The modeling showed that there should not be a rise in threading dislocation density. Microstructural investigations with TEM revealed that threading dislocations could be blocked by a two-dimensional defect we termed branch defects.[15] Figure 15 shows a plan-view TEM micrograph of branch defects, and some threading dislocations that have been trapped in them.

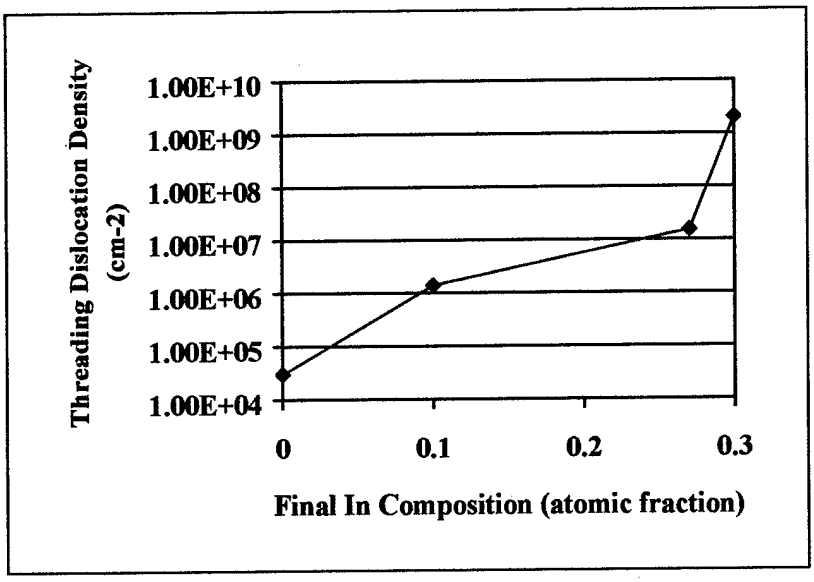


Figure 14: Rise in threading dislocation density as the final concentration of a graded layer is increased (grading rate (%In/μm held constant)

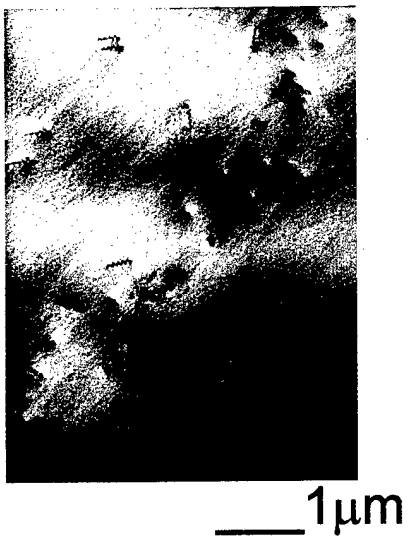


Figure 15: Plan-view TEM micrograph of wavy 'branch defects' in relaxed graded InGaP alloys on GaP substrates. The branch defects have strain fields that block threading dislocation motion, creating high threading dislocation densities. Note the number of sharper features (threading dislocations) trapped in the branch defects.

Fortunately, growth experiments were able to determine the frequency and strength of these defects as a function of growth temperature. Figure 16 plots the temperature range for a variety of graded buffer layers with different final In concentrations. By realizing that a single temperature cannot be chosen for the entire growth, we have employed a two-temperature optimization process that minimizes branch defect formation and maximizes dislocation flow. Figure 17 plots the improvement in threading dislocation density vs. final In composition in the graded relaxed InGaP buffer layer on GaP. By understanding the way that dislocations should flow during growth, and by using microstructural characterization to explore blocking effects on threading dislocations, we are able to produce LED-quality material in this system up to near 50% In.

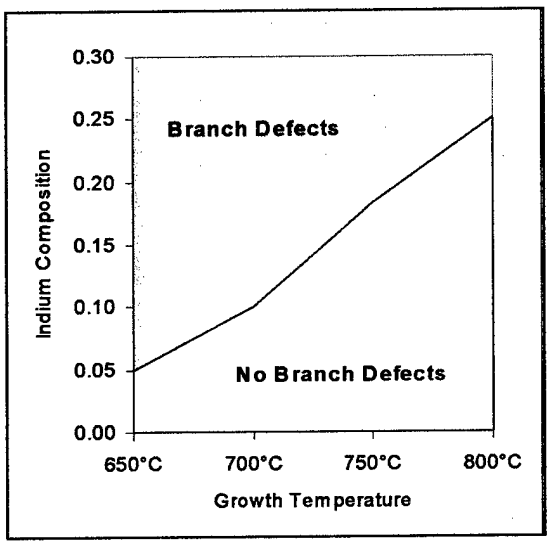


Figure 16: Graph showing the approximate regions of growth in which branch defects form in MOCVD relaxed InGaP graded layers on GaP substrates.

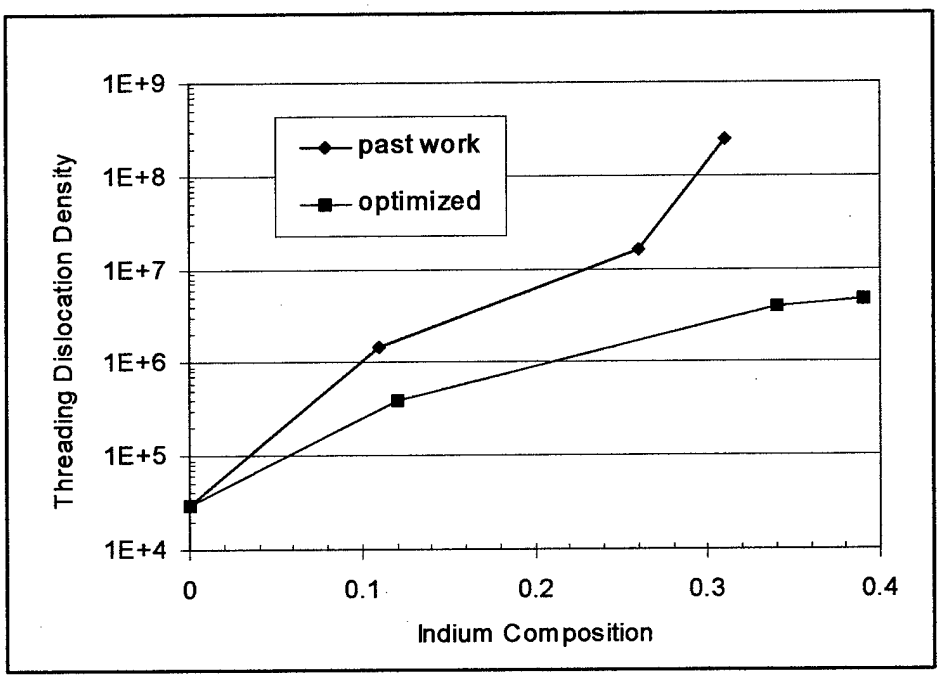


Figure 17: Plot of threading dislocation density in relaxed graded InGaP buffer layers on GaP substrates for different final In concentrations. Note the rapidly rising threading dislocation density has been subsided by using the two-step growth process to minimize branch defect formation.

5.7 III-V minority carrier devices on Si: solar cells and pn diodes. The advances in the materials science of III-V growth on graded GeSi elaborated above were immediately incorporated into a few types of devices, since (1) device measurements offered a vehicle by which we could assess electrical properties and, (2) the ultimate test of the relevance for our materials science advances is the demonstration of high quality III-V devices grown on Si using graded GeSi. Devices were grown by MBE and by MOCVD. Initially, much of the device work utilized MBE since this method allows a great deal of flexibility in device structure. GaAs pn diodes were grown and fabricated on GaAs, Ge and Ge/GeSi/Si substrates so that the impact of the substrate could be quantified. Figure 19 compares the I-V characteristics taken from 1 mm diameter mesa-isolated diodes, as a function of substrate material. Excellent and nearly identical I-V behaviors are observed, indicating that excellent diodes can be achieved on Ge/GeSi/Si substrates with quality comparable to diodes fabricated on GaAs and Ge substrates.[16]

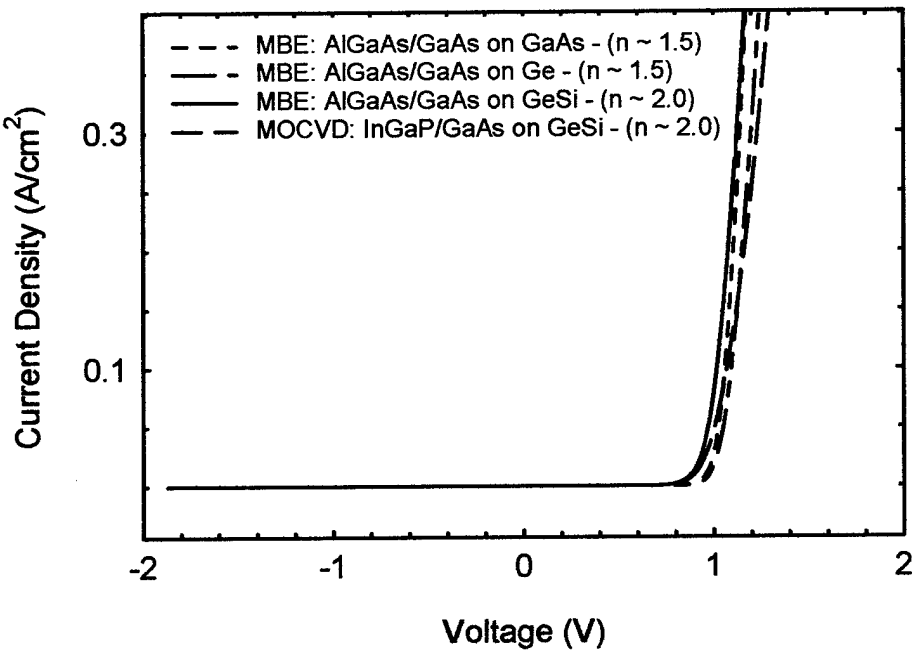


Figure 18: Dark I-V characteristics for GaAs pn homojunction diodes with either AlGaAs or InGaP window layers grown by MBE or MOCVD on GaAs, Ge and Ge/GeSi/Si substrates, as indicated. There is no change in reverse leakage current out to 2 volts, as seen, indicating the excellent diode properties have been achieved on the mismatched Ge/GeSi/Si substrates. The variation in forward current is due to contact variations and also due to an increase in ideality factor, as noted, for devices fabricated on the Ge/GeSi/Si substrates.

Since the ultimate device objective is the demonstration of high quality III-V *minority* carrier devices, considerable effort was expended toward this end. Figure 19 shows two types of GaAs solar cell structures grown on Ge/GeSi/Si substrates (same structures for diodes shown in Figure 18). The AlGaAs/GaAs pn cell structure was grown fully by MBE, whereas the InGaP/GaAs pn cell structure was grown using MBE to form an optimal GaAs/Ge interface and then transferred to an MOCVD reactor (courtesy of D. Wilt at NASA Glenn Research Center) where the solar cell growth was completed. Solar cells are excellent devices from which device

quality can be assessed, since they rely on the collection of photogenerated minority carriers but without the benefit of an applied field.

Figure 20 compares the external quantum efficiency (spectral response) characteristics of

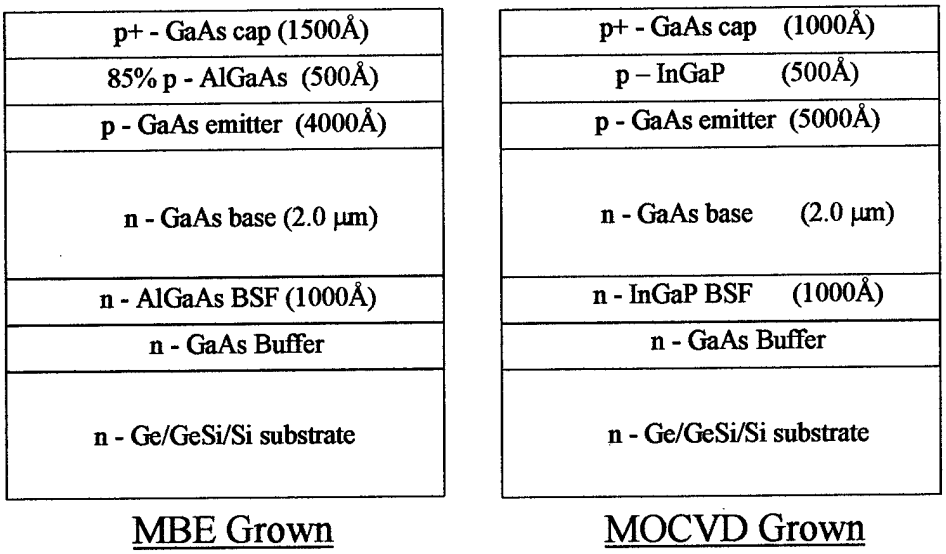


Figure 19: Device structures for MBE-grown AlGaAs/GaAs and MOCVD-grown InGaP/GaAs p^+n solar cells on Ge/GeSi/Si substrates

the AlGaAs/GaAs solar cells grown on GaAs, Ge and Ge/GeSi/Si substrates. Clearly, carrier collection is independent of substrate, which is significant from several perspectives. First, the high carrier lifetime (hence diffusion length) is maintained after complete device fabrication, indicating the robust nature of our growth methodology. Second, this shows that the residual TDD in the GaAs is indeed low enough to support devices having very high performance. Similar results were found for the InGaP/GaAs solar cell structures grown by MBE-MOCVD. In fact, Figure 21 shows the light I-V response of the InGaP/GaAs solar cell grown on Ge/GeSi/Si compared to the same structure grown on a Ge wafer substrate. Note that the cell performance parameters (inset in the figure) are virtually identical (although both are somewhat lower than expected due to a problem in the emitter doping and anti-reflection coating used for these runs). The Voc value is particularly noteworthy, since this parameter is very sensitive to defect-mediated recombination losses and historically has been poor for all prior attempts to develop a GaAs solar cell on Si. Our maximum published Voc value of 980 mV is the highest ever reported for a single junction GaAs cell grown on a Si substrate, and is directly related to our defect suppression methodology.[17] This is not an isolated result, however, and the histogram in Figure 22 shows the Voc distribution over several 10's of devices fabricated so far. Some very recent (yet to be published work in our group) has extended this value to 1048 mV (equivalent to values for homoepitaxial cells grown on GaAs substrates), with AM0 efficiencies greater than 17%.

Efficiencies of 20% are expected soon as our anti-reflection coating technology, which is currently limiting the current output of the cells (and is not related to the semiconductor material quality) becomes optimized. It is noteworthy that prior to our work, the highest reported Voc value for GaAs cells on Si was 940 mV (AM0) for but a single device. This limit has clearly been overcome due to the use of GeSi buffers to alleviate the mismatch between the GaAs and Si materials, rather than the various III-V graded buffer or superlattice approaches employed by other groups over the past 20 years.[18][19][20] These results are very clear demonstrations of the promise and potential presented by our approach toward integration of highly dissimilar materials. This provides a critical jump point for our proposed work, described later in this proposal.

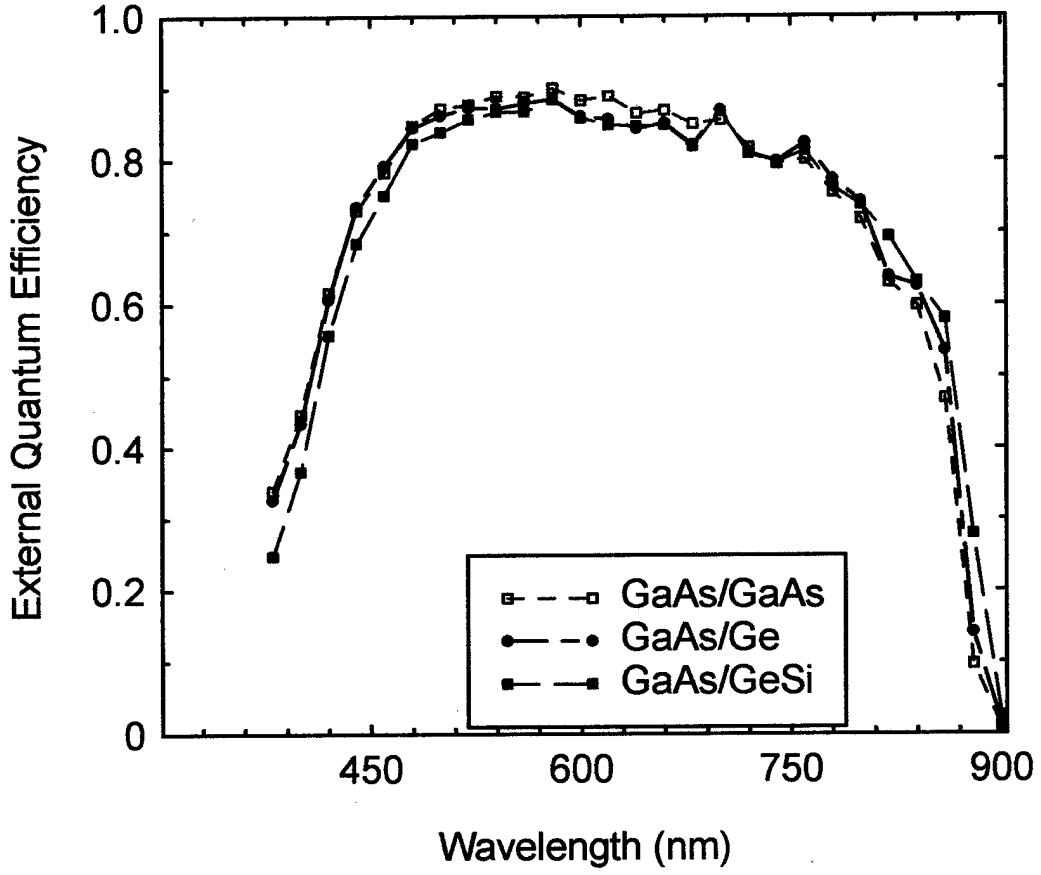


Figure 20: External quantum efficiency measurements (AM0) for single junction AlGaAs/GaAs cells grown by MBE on GaAs, Ge and Ge/GeSi/Si substrates indicating the similar minority carrier collection efficiency for each.

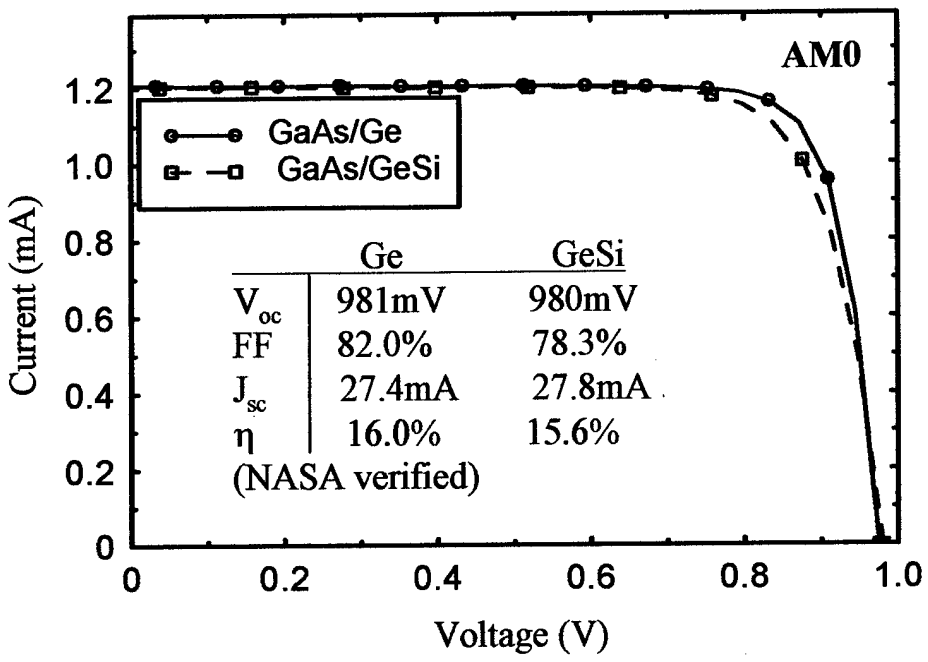


Figure 21: Light I-V response under AM0 conditions for representative single junction InGaP/GaAs cell (0.2 x 0.2 cm^2) grown on Ge/GeSi/Si substrates (courtesy of NASA Glenn Research Center).

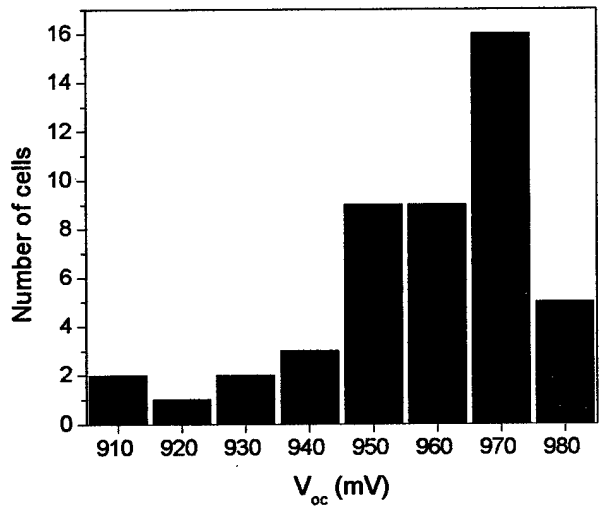


Figure 22: Histogram of Voc (AM0) distribution obtained for 2 x 2 mm^2 cells distributed across a large area (~7 cm^2) Ge/GeSi/Si substrate. The highest Voc value previously reported for single junction GaAs cells on Si was 0.95 V. Our recent, unpublished work has shifted this histrogram distribution toward yet higher values by ~ 60 mV.

5.8 InGaP transparent substrate LEDs The advances in InGaP graded buffer quality described previously in this summary allowed us to fabricate the first transparent visible LEDs without a wafer-bonding process. We have termed the all-epitaxial method as the epitaxial transparent substrate (ETS). The generic structure of the homojunction LEDs is just a GaP substrate (10 degrees off-cut), followed by an InGaP graded layer, followed by a uniform composition layer with a p-i-n structure formed in the uniform composition layer. Although not as efficient as a heterojunction LED, it is a simple beginning structure to explore. These LEDs show the expected trend for high quality relaxed buffers, in which the luminescence efficiency continues to increase with increasing In concentration. The LEDs also show that the half-width of the visible emission is the most narrow ever produced, again confirming high-quality material.[21] Visible ETS LEDs in operation show emission is occurring from all facets of the LED cube, confirming that the ETS structure has a transparent susbtrate.

6. Publications, Presentations

Journal Papers

1. J.A. Carlin, S.A. Ringel J.J. Boeckl, R.J. Kaplar and E.A. Fitzgerald, *"High lifetime GaAs on Si using GeSi buffers and its potential for space applications,"* Solar Energy Materials and Solar Cells vol. 66, pp. 621-630 (2001).
2. M. T. Currie, C. W. Leitz, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and D. A. Antoniadis, *"Carrier Mobilities and Process Stability of Strained Si n- and p- MOSFETs on SiGe Virtual Substrates"*, J. Vac. Sci. Technol. B, vol. 19, no. 6, pp. 2268-2279, (2001).
3. Z.-Y. Cheng, G. Taraschi, M. T. Currie, C. W. Leitz, M. L. Lee, A. J. Pitera, T. A. Langdo, J. L. Hoyt, D. A. Antoniadis, and E. A. Fitzgerald, *"Relaxed Silicon-Germanium on Insulator Substrate by Layer Transfer"*, J. Electron. Mater., vol. 30, no. 12, pp. L37-L39, (2001).
4. J. T. Borenstein, N. D. Gerrish, R. White, M. T. Currie, and E. A. Fitzgerald, *"Silicon Germanium Epitaxy: A New Material for MEMS"*, Materials Science of Microelectromechanical System (MEMS) Devices III, Mater. Res. Soc. Symp. Proc., vol. 657, pp. EE7.4.1-EE7.4.6, (2001)
5. W. Leitz, M. T. Currie, M. L. Lee, Z.-Y. Cheng, D. A. Antoniadis, and E. A. Fitzgerald, *"Hole Mobility Enhancements in Strained Si/$Si_{1-y}Ge_y$ p-Type Metal-Oxide-Semiconductor Field-Effect Transistors Grown on Relaxed $Si_{1-x}Ge_x$ ($x < y$) Virtual Substrates"*, Appl. Phys. Lett., vol. 79, no. 25, pp. 4246-4248, (2001)
6. Z.-Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, A. Pitera, M. L. Lee, T. A. Langdo, J. L. Hoyt, D. A. Antoniadis, and E. A. Fitzgerald, *"SiGe-On-Insulator (SGOI): Substrate Preparation and MOSFET Fabrication for Electron Mobility Evaluation"*, Technical Digest of the 27th IEEE International SOI Conference, pp. 13-14, 2001)
7. M. L. Lee, C. W. Leitz, Z.-Y. Cheng, A. Pitera, T. A. Langdo, M. T. Currie, G. Taraschi, E. A. Fitzgerald, and D. A. Antoniadis, *"Strained Ge Channel p-type Metal-Oxide-Semiconductor Field-Effect Transistors Grown on $Si_{1-x}Ge_x$/Si Virtual Substrates"*, Appl. Phys. Lett., vol. 79, no. 20, pp. 3344-3346, (2001)

8. C. S. Tan, W. K. Choi, L. K. Bera, K. L. Pey, D. A. Antoniadis, E. A. Fitzgerald, M. T. Currie, and C. K. Maiti, *"N_2O Oxidation of Strained-Si/Relaxed-SiGe Heterostructure Grown by UHVCVD"*, Solid-State Electronics, vol. 45, no. 11, pp. 1945-1949, (2001).
9. G. Taraschi, Z.-Y. Cheng, M. T. Currie, C. W. Leitz, T. A. Langdo, M. L. Lee, A. Pitera, E. A. Fitzgerald, D. A. Antoniadis, and J.L. Hoyt, *"Relaxed SiGe On Insulator Fabricated via Wafer Bonding and Layer Transfer: Etch-Back and Smart-cut Alternatives"*, Proceedings of the Tenth International Symposium on Silicon-on-Insulator Technology and Devices, Electrochem. Soc., pp. 27-32, (2001)
10. W. Leitz, M. T. Currie, A. Y. Kim, J. Lai, E. Robbins, E. A. Fitzgerald, and M. T. Bulsara, *"Dislocation Glide and Blocking Kinetics in Compositionally Graded SiGe/Si"*, J. Appl. Phys., vol. 90, no. 6, pp. 2730-2736, (2001)
11. Z.-Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, *"Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates"*, IEEE Electron Dev. Lett., vol. 22, no. 7, pp. 321-323, (2001).
12. A. Fitzgerald, M. T. Currie, C. W. Leitz, M. A. Armstrong, G. Taraschi, Z.-Y. Cheng, D. A. Antoniadis, C. S. Tan, S. Chattopadhyay, H. Zhao, P. S. Lee, L. Miao, S. J. Chua, K. L. Pey, and W. K. Choi, *"The Relaxed SiGe Materials Platform: Strained Si MOS"*, Proceedings of the 1st Singapore-MIT Alliance Annual Symposium, pp. B01.1-B01.14, (2001).
13. Y. Miron, C.W. Leitz, M.T. Currie, E.A. Fitzgerald, *"Characterization of the Reaction Between a Bilayer of Co/Zr to Relaxed $Si_{1-x}Ge_x$*, submitted to *Thin Solid Films*.
14. J.A. Carlin, S.A. Ringel, E.A. Fitzgerald, M. Bulsara and B.M. Keyes, "*Impact of GaAs buffer thickness on electronic quality of GaAs grown on graded Ge/GeSi/Si substrates*," Applied Physics Letters vol. 76, pp. 1884-1886, 2000.
15. G.Taraschi, T. A. Langdo, M. T. Currie, C. W. Leitz, M. L. Lee, J. Lai, K. Wu, and E. A. Fitzgerald, *"SiGe- on-insulator fabricated by wafer bonding and etch-back"*, 42nd 2000 Electronic MaterialsConference University of Denver, CO, June 21-23, (2000).
16. T. A. Langdo, C. W. Leitz, M. T. Currie, E. A. Fitzgerald, T. Lochtefeld, and D. A. Antoniadis, *"High Quality Ge on Si by Epitaxial Necking"*, Appl. Phys. Lett., vol. 76, no. 25, pp. 3700-3702, (2000)
17. S. A. Ringel, J. A. Carlin, C. W. Leitz, M. T. Currie, T. A. Langdo, E. A. Fitzgerald, M. T. Bulsara, D. M. Wilt, and E. V. Clark, *"III-V Space Solar Cells on Si Substrates Using Graded GeSi Buffers"*, Technical Digest of the 16th European Photovoltaic Solar Energy Conference and Exhibition, Glasgow, Scotland, May 1-5 (2000).
18. J. A. Carlin, M. K. Hudait, S. A. Ringel, D. M. Wilt, E. B. Clark, C. W. Leitz, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, *"High Efficiency GaAs-on-Si Solar Cells with High V_{oc} Using Graded GeSi Buffers"*, Conference Record of the 28th IEEE Photovoltaic Specialists Conference, pp. 1006-1011, (2000)
19. T. Hackbarth, H.-J. Herzog, M. Zeuner, G. Hock, E.A. Fitzgerald, M. Bulsara, C. Rosenblad, and H. von Kanel, *"Alternatives to Thick MBE-grown Relaxed SiGe Buffers"*, Thin Solid Films 369, 148 , (2000)
20. A.Y. Kim, M.E. Groenert, and E.A. Fitzgerald, *"Visible Light-emitting Diodes Grown on Optimized Graded InGaP/GaP Epitaxial Transparent Substrates with Controlled Dislocation Density"*, J. Electr. Mat. 29, L9 (2000).

21. S.M. Ting and E.A. Fitzgerald, *"Metal-organic Chemical Vapor Deposition of Single Domain GaAs on Ge/GeSi/Si and Ge Substrates"*, J. Appl. Phys. 87, 2618 (2000).
22. J.A. Carlin, S.A. Ringel, E.A. Fitzgerald and M. Bulsara, *High Quality GaAs growth by MBE on Si using GeSi buffers and prospects for space photovoltaics,"* **(Invited)**, Progress in Photovoltaics: Research and Applications vol. 8, pp. 323-332, 2000.
23. Q. Xu, J.W.P. Hsu, J.A. Carlin, R.M. Sieg, J.J. Boeckl and S.A. Ringel, *"Topographic and electronic studies of wedge-shape surface defects on AlGaAs/GaAs films grown on Ge substrates,"* Applied Physics Letters vol. 75, pp. 2111-2113, 1999.
24. E.A. Fitzgerald, A.Y. Kim, M.T. Currie, T.A. Langdo, G. Taraschi, M.T. Bulsara, *"Dislocation Dynamics in Relaxed Graded Composition Semiconductors"*, **(Invited)**, Materials Sci. Eng. Reports B67, 53 (1999).
25. A.Y. Kim W.S. McCullough, and E.A. Fitzgerald, *"Evolution of Microstructure and Dislocation Dynamics in $In_xGa_{1-x}P$ Graded Buffers Grown on GaP by MOVPE: Engineering Device-Quality Substrate Materials"*, J. Vac. Sci. Tech. B 17 (1999).
26. E.A. Fitzgerald, M.T. Currie, S.B. Samavedam, T.A. Langdo, G. Taraschi, V. Yang, C.W. Leitz, and M.T. Bulsara, *"Dislocations in Relaxed SiGe/Si Heterostructures"*, **(Invited)**, Phys. Stat. Sol. (a) 171, 227 (1999).
27. Y. Kim, E. A. Fitzgerald, *"Optimization of Microstructure and Dislocation Dynamics in In/sub x/Ga/sub 1-x/P Graded Buffers Grown on GaP by MOVPE, III-V and IV-IV Materials and Processing Challenges for Highly Integrated Microelectronics and Optoelectronics"*, Symposium Materials Res. Soc, pp.27-32, (1999)
28. E. A. Fitzgerald, A. Y. Kim, M. T. Bulsara, and M. T. Currie, *"Dislocation Dynamics in Graded Relaxed SiGe/Si, InGaAs/GaAs, and InGaP/GaP"*, Inst. Phys. Conf. Ser. No. 164, Proceedings of the Microscopy of Semiconductor Materials Conference, pp. 259-268, (1999)
29. E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, S. B. Samavedam, and T. A. Langdo, *"Relaxed Graded Buffer Layers in the SiGe/Si and InGaAs/GaAs Materials Systems"*, Proceedings of the First International Workshop on Lattice Mismatched Thin Films, TMS, pp. 63-71, (1999)
30. C. Ferrari, S. Gennari, G. Salviati, M. Natali, G. Drigo, G. Rossetto, M. T. Currie, and E. A. Fitzgerald, *"X-Ray Topographic Analysis of Misfit Dislocation Distribution in InGaAs and GeSi/Si Partially Relaxed Heterostructures"*, Proceedings of the First International Workshop on Lattice Mismatched Thin Films, TMS, pp. 39-46, (1999).
31. J. T. Borenstein, N. D. Gerrish, M. T. Currie, and E. A. Fitzgerald, *"A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining"*, Technical Digest of the Twelfth IEEE International Conference on Micro Electro Mechanical Systems, pp. 205-210, (1999)
32. J. T. Borenstein, N. D. Gerrish, M. T. Currie, and E. A. Fitzgerald, *"Etch Selectivity of Novel Epitaxial Layers for Bulk Micromachining"*, in Materials Science of Microelectromechanical Systems (MEMS) Devices, Mater. Res. Soc. Symp. Proc., vol. 546, pp. 69-74, (1999).
33. S. M. Ting, M. B. Bulsara, V. K. Yang, M. Groenert, S. B. Samavedam, M. T. Currie, T. A. Langdo, E. A. Fitzgerald, A. Joshi, R. Brown, X. Wang, R. M. Sieg, and S. A. Ringel, *"Monolithic Integration of III-V Materials and Devices on Silicon"*, Proceedings of the SPIE, vol. 3630, pp. 19-28, (1999)

34. S. M. Ting, M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, *"Low Defect Density GaAs Grown on Compositionally-Graded Ge/Ge_xSi_{1-x}/Si Substrates"*, submitted for publication 7/99
35. S. M. Ting and E. A. Fitzgerald, *"Metal-Organic Chemical Vapor Deposition of Single-Domain GaAs on Ge and Ge/Ge_xSi_{1-x}/Si Substrates"*, accepted for publication, *Journal of Applied Physics*.
36. R.M. Sieg, J.A. Carlin, J.J. Boeckl, S.A. Ringel, M.T. Currie, S.M. Ting, T.A. Langdo, G. Taraschi, E.A. Fitzgerald and B.M. Keyes, *"High Minority-Carrier Lifetimes in GaAs Grown on Low-Defect-Density Ge/GeSi/Si Substrates,"* Appl. Phys. Lett. 73, 3111-3113, 1998.
37. E.A. Fitzgerald and L. C. Kimerling, *"Silicon-Based Microphotonics and Integrated Optoelectronics"*, **(Invited)**, MRS Bulletin 23, 39 (1998).
38. Q. Xu, J.W.P. Hsu, S.M. Ting, E.A. Fitzgerald, R.M. Sieg and S.A. Ringel, *"Scanning Force Microscopy Study of GaAs Films Grown on Offcut Ge Substrates,"* J. Electron. Mat., 1010-1016, 1998.
39. S. B. Samavedam, M. T. Currie, T. A. Langdo, and E.A. Fitzgerald, *"High-quality germanium photodiodes integrated on silicon substrates using optimized relaxed graded buffers"*, Applied Physical Letters 73, 2125(1998).
40. S.M. Ting, E.A. Fitzgerald, R.M. Sieg and S.A. Ringel, *"Range of Defect Morphologies on GaAs Grown on Offcut (001) Ge Substrates"*, J. Electron Mat., 27, 451-461, 1998.
41. R.M. Sieg, S.A. Ringel, S.M. Ting and E.A. Fitzgerald, and R.N. Sacks, *"Anti-Phase Domain-Free Growth of GaAs on offcut (001) Ge Substrates by Molecular Beam Epitaxy With Suppressed Ge Outdiffusion,"* J. Electron. Mat. 27, 900-907, 1998.
42. M.T. Currie, S.B. Samavedam, T.A. Langdo, C.W. Leitz, and E.A. Fitzgerald, *"Controlling Threading Dislocation Densities in Ge on Si Using Graded GeSi Layers and Chemical-Mechanical Polishing"*, Applied Physics Letters 72, 1718 (1998).
43. J.A. Carlin, S.A. Ringel, R.N. Sacks, and K.S. Yap, *"Role of Al Content on Surface Structure Evolution of Low Temperature AlGaAs and its Effect on Critical Thickness,"* J. Vac. Sci. Tech. B16, 1998.
44. R.M. Sieg, S.A. Ringel, S.M. Ting, S.B. Samavedam, M. Currie, T. Landgo and E.A. Fitzgerald, *"Toward Device-Quality GaAs Growth on Offcut Ge/GeSi/Si Substrates,"* J. Vac. Sci. Tech. B16, 1471-1474, 1998.
45. S. A. Ringel, R. M. Sieg, J. A. Carlin, S. M. Ting, M. T. Currie, V. K. Yang, E. A. Fitzgerald, M. T. Bulsara, and B. M. Keyes, *"Toward Achieving Efficient III-V Space Cells on Ge/GeSi/Si Wafers"*, Proceedings of the 2nd World Conference and Exhibition on Photovoltaic Solar Energy Conversion, (1998)
46. R. M. Sieg, S. A. Ringel, S. M. Ting, S. B. Samavedam, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, *"Toward Device-Quality GaAs Growth by Molecular Beam Epitaxy on Offcut Ge/$Si_{1-x}Ge_x$/Si Substrates"*, J. Vac. Sci. Technol. B, vol. 16, no. 3, pp. 1471-1474, (1998)
47. S. B. Samavedam, M. T. Currie, T. A. Langdo, S. M. Ting, and E. A. Fitzgerald, *"Quality Germanium Photodiodes on Silicon Substrates using an Intermediate Chemical Mechanical Polishing Step, Materials and Devices for Silicon-Based Optoelectronics"*, Mater. Res. Soc. Symp. Proc., pp. 187-192, (1998)

48. E. A. Fitzgerald, K. C. Wu, M. T. Currie, N. D. Gerrish, D. Bruce, and J. T. Borenstein, *"Silicon-Based Epitaxial Films for MEMS, Microelectromechanical Structures for Materials Research"*, Mater. Res. Soc. Symp. Proc., vol. 518, pp. 233-238, (1998)
49. S. M. Ting, S. B. Samavedam, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, *"Suppression of Antiphase Disorder in GaAs Grown on Relaxed GeSi Buffers by Metal-Organic Chemical Vapor Deposition, Defect and Impurity Engineered Semiconductors II"*, Mater. Res. Soc. Symp. Proc., vol. 510, pp. 107-112, (1998)
50. M.T. Bulsara, C. Leitz, and E.A. Fitzgerald, *"Relaxed $In_xGa_{1-x}As$ Graded Buffers Grown with Organometallic Vapor Phase Epitaxy on GaAs"*, *Applied Physics Letters* **72**, 1608, (1998)
51. A.M. Joshi, R. Brown, X. Wang, S. Ting, M. Bulsara, and E.A. Fitzgerald, *"Monolithic InGaAs on Si Short Wave Infrared Detector Arrays"*, SPIE Proceedings 2999, 211 , (1997)

Conference Papers and Presentations

1. S.A. Ringel, J.A.Carlin*, C.L. Andre,* J. Boeckl,* C.W. Leitz,* M. Currie,* T. Langdo,* E.A. Fitzgerald, A. Allerman, D.M. Wilt and E.B. Clark *"Development of High Efficiency GaAs-on-Si Solar Cells Using GeSi Interlayers,"*, Space Power Workshop **(Invited)**, Redondo Beach, CA, 2001.
2. Lisa McGill, Eugene Fitzgerald, Steve Stockman, James Huang, Pat Grillot, Sung Soo-Yi, Andrew Kim, *"Visible LED Materials Based on Relaxed, Graded InGaP: Engineering High Performance in the Presence of Defects"*, 2001 Electronic Materials Conference, 2001
3. C. W. Leitz, M. T. Currie, E. A. Fitzgerald, and D. A. Antoniadis, *"Investigating Hole Mobility Enhancements in Surface Strained Si/SiGe Heterostructures"*, 43rd Electronic Materials Conference, Notre Dame, Indiana, June 2001
4. C.W. Leitz, M.T. Currie, M.L. Lee, Z. Cheng, D.A. Antoniadis, and E.A. Fitzgerald, *"Optimized Heterostructures for SiGe-based CMOS Applications"*, Fall 2001 Materials Research Society Conference, proceedings in print, 2001
5. M.L. Lee, C.W. Leitz, A. Pitera, G. Taraschi, D. Antoniadis, and E. Fitzgerald, *"Strained-Germanium Channel p-Type MOSFETs Fabricated on $Si_{1-x}Ge_x$ Virtual Substrates"*, Fall 2001 Materials Research Society Conference, proceedings in print, 2001
6. Z-Y. Cheng, M.T. Currie, C.W. Leitz, G. Taraschi, A. Pitera, M.L. Lee, T.A. Langdo, J.L. Hoyt, D.A. Antoniadis, and E.A. Fitzgerald, *"Silicon-Germanium on Insulator (SGOI)"*, Fall 2001 Materials Research Society Conference, proceedings in print, 2001
7. M. Groenert, V. Yang, M. Currie, C. Leitz, and E. Fitzgerald, *"Strategies for Direct Monolithic Integration of $Al_xGa_{(1-x)}As/In_xGa_{(1-x)}As$ LEDs and Lasers on Ge/GeSi/Si Substrates Via Relaxed Graded $Ge_xSi_{(1-x)}$ Buffer Layers"*, Fall 2001 Materials Research Society Conference, proceedings in print., 2001
8. S. Eguchi, J.L. Hoyt, C.W. Leitz, and E.A. Fitzgerald, *"Behavior of Ion-Implanted n-Type Dopants in Silicon-Germanium"*, Fall 2001 Materials Research Society Conference, proceedings in print, 2001
9. Z-Y. Cheng, M.T. Currie, C.W. Leitz, G. Taraschi, A. Pitera, M.L. Lee, T.A. Langdo, J.L. Hoyt, D.A. Antoniadis, and E.A. Fitzgerald, *"SiGe-on-Insulator (SGOI): Substrate Preparation and MOSFET Fabrication for Electron Mobility Evaluation"*, Proceedings of the 2001 IEEE International SOI Conference, 13, 2001

10. G.Taraschi, Z-Y. Cheng, M.T. Currie, C.W. Leitz, T.A. Langdo, M.L. Lee, A. Pitera, E.A. Fitzgerald, J.L. Hoyt, and D.A. Antoniadis, *"Relaxed SiGe on Insulator Fabricated Via Wafer Bonding and Layer Transfer: Etch-Back and Smart-Cut Alternatives"*, Proceedings of the 10th ECS International Conference on SOI, 27, 2001
11. C.W. Leitz, M.T. Currie, M.L. Lee, D.A. Antoniadis, and E.A. Fitzgerald, *"Investigating Hole Mobility Enhancements in Surface Strained Si/SiGe Heterostructures"*, Electronic Materials Conference, 2001
12. V. Yang, M. Groenert, S. Ting, M. Bulsara, M. Currie, C. Leitz, A. Pitera, G. Taraschi, Z-Y. Cheng, and E. Fitzgerald, *"Characterization and Fabrication of Optical Devices on SiGe Virtual Substrates"*, Fall 2001 Materials Research Society Conference, 2001
13. S. Eguchi, H. Nayfeh, C.W. Leitz, E.A. Fitzgerald, and J.L. Hoyt, *"Diffusion of Ion Implanted n-Type Dopants in Silicon-Germanium Alloys"*, Electronic Materials Conference, 2001
14. J.A. Carlin, M.K. Hudait, S.A. Ringel, D. Wilt, E. Clark, C.W. Leitz, M. Currie, T. Langdo and E.A. Fitzgerald, *"High Efficiency GaAs-on-Si Solar Cells With High V_{oc} using Graded GeSi Buffers,"* Proc., IEEE Photovoltaic Specialists Conference, Anchorage, AK,, pp. 1006-1011, 2000.
15. M.T. Currie, C.W. Leitz, T.A. Langdo, E.A. Fitzgerald, M.A. Armstrong, D.A. Antoniadis, *"Carrier Mobilities and Process Stability of n- and p- Surface Channel Strained Si/SiGe MOSFETs"*, TMS/IEEE Electronic Materials Conference, Denver, 2000.
16. C.L. Andre, J.J. Boeckl, S.A. Ringel, C.W. Leitz, M.T. Currie, T.A. Langdo, E.A. Fitzgerald and D.M. Wilt, *"Low-Temperature GaAs films grown on Ge and GE/Ge-Si substrates*, TMS/IEEE Electronic Materials Conference, Denver, 2000.
17. A.Y. Kim and E.A. Fitzgerald, *"Dislocation Dynamics Explored via Analysis of Reciprocal Space Maps in Lattice-Mismatched Semiconductor Heterostructures"*, TMS/IEEE Electronic Materials Conference, Denver, 2000.
18. G. Taraschi, T.A. Langdo, M.T. Currie, C.W. Leitz, M.L. Lee, D.A. Antoniadis, E.A. Fitzgerald, *"SiGe On Insulator Fabricated by Wafer Bonding and Etch-back"*, TMS/IEEE Electronic Materials Conference, Denver, 2000.
19. C.W. Leitz, M.T. Currie, A.Y. Kim, S.B. Samavedam, J. Lai, E. Robbins, E.A. Fitzgerald, and M.T. Bulsara, *"Dislocation Glide, Blocking, and Reduction Kinetics in Compositionally Graded SiGe"*, TMS/IEEE Electronic Materials Conference, Denver, 2000.
20. C.L. Andre, J.J. Boeckl, S.A. Ringel, C.W. Leitz, M.T. Currie, T.A. Langdo, E.A. Fitzgerald and D.M. Wilt, *"Low-Temperature GaAs films grown on Ge and Ge/Ge-Si substrates,"* TMS/IEEE Electronic Materials Conference, Denver, 2000.
21. E.A. Fitzgerald, *"Dislocation Flow in Lattice-Mismatched Semiconductor Films"*, Gordon Conference on Thin Film Mechanics, Plymouth, NH, July 2000. **(Invited)**
22. S.A. Ringel, J.A. Carlin, C. Andre, R. Sacks, E.A. Fitzgerald, M. Currie, T. Langdo and C. Leitz, *"Epitaxial integration of III-V materials and devices with Si using graded GeSi buffers,"* IEEE/LEOS International Symposium on Compound Semiconductors (ISCS), Monterey CA, **Invited** (2000).
23. S.A. Ringel, J.A. Carlin, C.W. Leitz, M. Currie, T. Langdo, E.A. Fitzgerald, D.M. Wilt and E.V. Clark, *"III-V space solar cells on Si substrates using graded GeSi buffers,"* **Plenary**, 16th European Photovoltaic Solar Energy Conference, Glasgow, pp.939-944 (2000).

24. Andrew Kim, Lisa McGill, Eugene Fitzgerald, *"Evolution of Microstructure in Strain-relaxed InGaP Films Grown by MOVPE"*, 2000 Spring MRS Conference, 2000
25. J.A. Carlin, M.K. Hudait, S.A. Ringel, D.M. Wilt, E.B. Clark, C.W. Leitz, M.T. Currie, T. Langdo, and E.A. Fitzgerald, *"High efficiency GaAs-on-Si Solar Cells with High V_{oc} Using Graded GeSi Buffers"*, Proceedings of the 28th IEEE Photovoltaic Specialists Conference, 1006, 2000
26. C. S. Tan, W. K. Choi, L. K. Bera, K. L. Pey, D. A. Antoniadis, E. A. Fitzgerald, M. T. Currie, and C. K. Maiti, *"N_2O Oxidation of Strained-Si/Relaxed-SiGe Heterostructure Grown by UHVCVD"*, International Conference on Communications, Computers, and Devices, Kharagpur, India, December 2000
27. S.A. Ringel, J.A. Carlin, J.J. Boeckl, R.J. Kaplar and E.A. Fitzgerald, *"High lifetime GaAs on Si using GeSi buffers and its potential for space applications,"* Proc. 14th Photovoltaic Science and Engineering Conference, Sapporo Japan, pp. 605-606, 1999.
28. A.Y. Kim and E.A. Fitzgerald, *"Engineering High-Quality InGaP Graded Composition Buffers on GaP for Transparent Substrate Light-Emitting Diodes"*, SPIE 3621, 179 (1999).
29. S.A. Ringel, J.A. Carlin, R.M. Sieg, J.J. Boeckl and E.A. Fitzgerald, *"Highly controlled GaAs/Ge interfaces and implications for III-V optoelectronic integration onto group IV substrates,"* Engineering Foundation Conference on Lattice-Mismatched and Heterovalent Epitaxy, **(Invited)** Barga, Italy, 1998; Lattice Mismatched Thin Films vol 1, pp. 87-96, 1999.
30. E.A. Fitzgerald, M.T. Bulsara, M.T. Currie, S.B. Samavedam, and T.A. Langdo, *"Relaxed Graded Buffer Layers in the SiGe/Si and InGaAs/GaAs Materials Systems"*, Engineering Foundation Conference on Lattice-Mismatched and Heterovalent Epitaxy, Barga, Italy, 1998; Lattice Mismatched Thin Films vol 1, 63, 1999.
31. E.A. Fitzgerald, *" Building a SiGe Materials Bridge between GaAs and Si"*, National Univeristy of Singapore, Singapore, January 1999. **(Invited)**
32. E.A. Fitzgerald, *"Relaxed Graded Semiconductors"*, Lawrence Symposium on Epitaxy, Phoenix, AZ, January 1999. **(Invited)**
33. S.M. Ting, M.T. Bulsara, V. Yang, M. Groenert, S.B. Samavedam, M.T. Currie, T.A. Langdo, E.A. Fitzgerald, A. Joshi, R. Brown, X. Wang, R.M. Sieg, S.A. Ringel, *"Monolithic Integration of III-V Materials and Devices on Si"*, SPIE 3630, 19 (1999).
34. E.A. Fitzgerald, *"Dislocation Dynamics in Graded Relaxed SiGe/Si, InGaAs/GaAs, and InGaP/GaP"*, Microscopy of Semiconductor Materials Conference, Oxford University, Oxford, UK, March 1999. **(Invited)**
35. J.A. Carlin, S.A. Ringel, E.A. Fitzgerald and M. Bulsara *"High Quality GaAs growth by MBE on Si using GeSi buffers and prospects for space photovoltaics,"* **(Invited)**, 15th Space Photovoltaics Research and Technology Conference, Cleveland OH, 1999.
36. E.A. Fitzgerald, *"Relaxed Graded Lattice-Mismatched Layers"*, Harvard University, Cambridge, MA, February 1999. **(Invited)**
37. Michael Groenert, V. Yang, J.A. Carlin, S. Ringel and E.A. Fitzgerald, *"AlGaAs and InGaAs-based Light Emitters on Si via Relaxed Graded GeSi Buffer Layers"*, 1999 Electronic Materials Conference, Santa Barbara, CA, June 26,1999
38. A.Y. Kim, E. A. Fitzgerald, *"Optimization of Microstructure and Dislocation Dynamics in In/sub x/Ga/sub 1-x/P Graded Buffers Grown on GaP by MOVPE, III-V and IV-IV*

Materials and Processing Challenges for Highly Integrated Microelectronics and Optoelectronics", Symposium Materials Res. Soc, (1999), pp.27-32, 1999

39. T. A. Langdo, M. T. Currie, G. Taraschi, and E. A. Fitzgerald, *"Selective SiGe Nanostructures Grown by UHVCVD"*, 41st Electronic Materials Conference, Santa Barbara, California, June 1999
40. Borenstein, J.T., Gerrish, N.D., Currie, M.T., and Fitzgerald, E.A, *"A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining"*, **Twelfth IEEE International Conference on Micro Electro Mechanical Systems, 1999, 205,** 1999
41. S.A. Ringel, R.M. Sieg and J.A. Carlin, *"Highly-Controlled GaAs/Ge Interfaces and Implications for III-V Cells on Si,"* **(Invited)**, Space Power Workshop, Long Beach, CA, 1998.
42. S.A. Ringel, R.M. Sieg, J.A. Carlin, S. Ting, M. Currie, V. Yang, E.A. Fitzgerald, M. Bulsara and B.M. Keyes, *"Toward Achieving Efficient III-V Space Cells on Ge/GeSi/Si Wafers,"* Proc. 2nd World Conf. and Exhib. on Photovoltaic and Solar Energy Conversion, Vienna, Austria, pp. 3594-3599, 1998.
43. A. Kim and E. Fitzgerald, *"Engineering Dislocation Dynamics in Inx(AlyGa1-y)1-xP Graded Buffers Grown on GaP by OMVPE"*, MRS Proceedings, 510, 131 (1998).
44. E.A. Fitzgerald, "Dislocations in Relaxed SiGe", Extended Defects in Semiconductors Conference, Poland, September 1998. **(Invited)**
45. S.M. Ting, E.A. Fitzgerald et al., *"Suppression of Antiphase Disorder in GaAs Grown on Relaxed SiGe Buffers by Metal-Organic Chemical Vapor Deposition"*, MRS Proceedings 510, (1998).
46. E.A. Fitzgerald, *"Building a SiGe Bridge between GaAs and Si"*, Brown University, November 1998. **(Invited)**
47. E.A. Fitzgerald, *"Controlling Dislocations in SiGe/Si"*, Gordon Conference on Point and Line Defects in Semiconductors, New London, NH, July 1998. **(Invited)**
48. S. M. Ting, S. B. Samavedam, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, *"Suppression of Antiphase Disorder in GaAs Grown on Relaxed GeSi Buffers by Metal-Organic Chemical Vapor Deposition"*, Spring Materials Research Society Meeting, 1998
49. M.T. Bulsara and E.A. Fitzgerald, "High quality InxGa1-x/As heterostructures grown on GaAs with MOVPE", Proceedings for Fall MRS 1998, Impurity Engineered Semiconductors II. Symposium, 101, 1998
50. M.T. Bulsara, C. Leitz, and E.A. Fitzgerald, *"Relaxed $In_xGa_{1-x}As$ Graded Buffers Grown with Organometallic Vapor Phase Epitaxy on GaAs"*, Materials Research Society Conference Proceedings **484**, 631, 1998
51. E.A. Fitzgerald, *"Applications of Relaxed SiGe layers"*, Applied Materials Epitaxy Conference, Portland, OR, February 1999. **(Invited)**
52. R.M. Sieg, S.A. Ringel, S.M. Ting, S.B. Samavedam, M. Currie, T. Langdo and E.A. Fitzgerald, *"Toward Device-Quality GaAs Growth by MBE on Offcut $Ge/Si_{1-x}Ge_x/Si$ Substrates,"* 16th North American Conf. On Molecular Beam Epitaxy, Ann Arbor, MI, 1997.
53. J.A. Carlin, S.A. Ringel and R.N. Sacks, *"Role of Al Content on Surface Roughening and Critical Thickness of Low Temperature $Al_xGa_{1-x}As$,"* 16th North American Conf. On Molecular Beam Epitaxy, Ann Arbor, MI, 1997.

54. S.B. Samavedam, M.T. Currie, T.A. Langdo, S.M. Ting and E.A. Fitzgerald, *"Materials Issues in the Integration of Ge Photodetectors on Si Substrates"*, Proceedings for Fall MRS 1997, Dec. 1997.
55. S.A. Ringel, R.M. Sieg, S.M. Ting and E.A. Fitzgerald, *"Anti-Phase Domain-Free GaAs on Ge Substrates Grown by Molecular Beam Epitaxy for Space Solar Cell Applications,"* **Area Plenary Presentation**, Proc. 26th IEEE Photovoltaic Specialists Conf., Anaheim, CA, pp. 793-798, 1997.
56. R.M. Sieg, S.A. Ringel, S.M. Ting and E.A. Fitzgerald, *"Device-Quality Gallium Arsenide Grown on Offcut Ge Substrates by Molecular Beam Epitaxy for Solar Cells,"* Fall MRS Meeting, Boston, MA, 1997.
57. S.M. Ting, E.A. Fitzgerald, R.M. Sieg and S.A. Ringel, *"Range of Defect Morphologies for GaAs Grown on Offcut Ge Substrates,"* 39th TMS/IEEE Electronic Materials Conference, Ft. Collins, CO,1997.
58. R.M. Sieg, S.A. Ringel, S.M. Ting and E.A. Fitzgerald, *"Anti-Phase Domain-Free GaAs Grown on Ge Substrates by Molecular Beam Epitaxy Using Either As or Ga Terminated Ge Surfaces,"* 39th TMS/IEEE Electronic Materials Conference, Ft. Collins, CO,1997.
59. Q. Xu, J.W.P. Hsu, S.M. Ting, E.A. Fitzgerald, R.M. Sieg and S.A. Ringel, *"Scanning Force Microscopy Study of GaAs Films Grown on Offcut Ge Substrates,"* 39th TMS/IEEE Electronic Materials Conference, Ft. Collins, CO,1997.
60. A.M. Joshi, R. Brown, X. Wang, S. Ting, M. Bulsara, and E.A. Fitzgerald, *"Monolithic InGaAs on Si Short Wave Infrared Detector Arrays"*, SPIE Proceedings 2999, 211 , (1997)
61. M.T. Bulsara, C. Leitz, and E.A. Fitzgerald, *"Relaxed InxGa1-xAs Graded Buffers Grown with Organometallic Vapor Phase Epitaxy on GaAs"*, Fall MRS , Dec. 1997

7. Student Progress and Success

The core program and 2 AASERT awards have been used to support 3 graduate students at Ohio State, and 2 graduate students (+2 DOD fellows) at MIT. Of the OSU students supported on this program, Dr. Robert M. Sieg graduated with a Ph.D. degree in 1998 and is now a postdoc at Sandia National Labs in the Compound Semiconductor Division, John A. Carlin has received his Ph.D. in 2001 and joined Amberwave Systems Corp. (a small company spun out of MIT by Fitzgerald to commercialize various aspects of the GeSi/Si substrate technology), and Carrie L. Andre is currently a Ph.D. student who is continuing on the new ARO program. At MIT, Dr. Steve Ting was supported initially in the program, and he is currently employed by EMCORE. MIT was fortunate to amplify the ARO funding with 2 DOD fellowships students, initially Dr. Andrew Kim, currently employed by LumiLEDs Lighting (spin-out of HP/Agilent for commercialization of high-brightness LEDs), and currently Lisa McGill, who should graduate in 2003-2004 timeframe. Andy was supported by the ARO program by salary after the fellowship ended, and we will be doing the same with Lisa. Matt Currie was supported by the ARO program when he was working on the relaxed SiGe portion of his thesis. Matt Currie has be graduated from MIT in 2001 and is currently employed by Amberwave Systems Corporation.

8. Inventions, Patents

Patents from work in program

1. US6107653: Controlling threading dislocation densities in Ge on Si using graded GeSi layers and planarization

2. Pending, Method of producing device quality (Al)InGaP alloys on lattice-matched substrates

9. Bibliography

[1] E.A. Fitzgerald, Y.-H. Xie, D. Monroe, P.J. Silvennan, J.-M. Kuo, A.R. Kortan, F.A. Thiel, B.E. Weir, and L.C. Feldman, J. Vac. Sci. Tech. B 10, 1807 (1992).

[2] S.B. Samavedam and E.A. Fitzgerald, J. Appl. Phys. 81, 3108 (1997).

[3] M.T. Currie, S.B. Samavedam, T.A. Langdo, C.W. Leitz, and E.A. Fitzgerald, Applied Physics Letters 72, 1718 (1998).

[4] E.A. Fitzgerald, A.Y. Kim, M.T. Currie, T.A. Langdo, G. Taraschi, M.T. Bulsara, Materials Science and Engineering B67, 53 (1999).

[5] R.M. Sieg, S.A. Ringel, S.M. Ting and E.A. Fitzgerald, and R.N. Sacks, J. Electron. Mat. **27**, 900 (1998).

[6] R.M. Sieg, S.A. Ringel, S.M. Ting, S.B. Samavedam, M. Currie, T. Landgo and E.A. Fitzgerald, J. Vac. Sci. Tech. **B16**, 1471 (1998).

[7] S.A. Ringel, J.A. Carlin, R.M. Sieg, J.J. Boeckl and E.A. Fitzgerald, Lattice Mismatched Thin Films **1**, 87 (1999).

[8] R.M. Sieg, J.A. Carlin, J.J. Boeckl, S.A. Ringel, M.T. Currie, S.M. Ting, T.A. Langdo, G. Taraschi, E.A. Fitzgerald and B.M. Keyes, Appl. Phys. Lett. **73**, 3111 (1998).

[9] J.A. Carlin, S.A. Ringel, E.A. Fitzgerald and M. Bulsara, Progress in Photovoltaics: Research and Applications **8**, 323 (2000).

[10] J.A. Carlin, S.A. Ringel, E.A. Fitzgerald, M. Bulsara and B.M. Keyes, Applied Physics Letters **76**, 1884 (2000).

[11] M. Yamaguchi and C. Amano, J. Appl. Phys. **58**, 3601 (1985).

[12] H. Kroemer, J. Crys. Growth 81, 193 (1987); D.K. Biegelsen, R.D. Bringans, and J.E. Northrup, Materials Science and Engineering B14, 317 (1992).

[13] S.M. Ting and E.A. Fitzgerald, J. Appl. Phys. 87, 2618 (2000).

[14] L.J. Stinson, J.G. Yu, S.D. Lester, M.J. Peanasky, K. Park, Appl. Phys. Lett. 58, 2012 (1991).

[15] A.Y. Kim W.S. McCullough, and E.A. Fitzgerald, J. Vac. Sci. Tech. B 17 (1999).

[16] S.A. Ringel, J.A. Carlin, J.J. Boeckl, R.J. Kaplar and E.A. Fitzgerald, Solar Energy Materials and Solar Cells, in press (2000).

[17] J.A. Carlin, S.A. Ringel, E. Clark, D. Wilt, E.A. Fitzgerald, and M. Bulsara, Proc. IEEE Photovoltaic Specialists Conference, Anchorage, AK, in press (2000).

[18] M. Yamaguchi, J. Mater. Res. **6**, 376 (1991).

[19]. R.K. Ahrenkiel, M.M. Al-Jassim, B. Keyes, D. Dunlavy, K.M. Jones, S.M. Vernon, and T.M. Dixon, J. Electrochem. Soc. **137**, 996 (1990).

[20] R. Venkatasubramanian, M.L. Timmons, J.B. Posthill, B.M. Keyes, and R.K. Ahrenkiel, J. Cryst. Growth **107**, 489 (1991).

[21] A.Y. Kim, M.E. Groenert, and E.A. Fitzgerald, J. Electr. Mat. 29, L9 (2000).

10. Appendix

A. Commercialization of ARO Basic Science Success

One measure of the success of the materials science achieved in the previous ARO program is the aggressive nature in which the investigators have pursued commercialization of the technology. Professor Fitzgerald has founded AmberWave LLC, which recently has transformed into AmberWave Systems Corporation. AmberWave Systems Corporation is commercializing the use of relaxed SiGe on Si substrates for fabrication of optoelectronic and electronic systems. The company has grown rapidly, receiving private seed funding in the fall of 1999 and closing a second round of financing in April 2000. The company has 22 hires, and also has received early SBIR funding which helped some of the earliest technology scale the university/company chasm. Professor Steven Ringel is an advisor to the company and has been a subcontractor on the early Phase I programs, and will be a subcontractor on the Phase II program. SBIR contracts aside, the company is market driven: total private capital expenditures in AmberWave will exceed government contributions by a factor of greater than 20:1.

In addition to the direct spin-out of Amberwave Systems, which is based on the main Ge/SiGe/Si focus of the ARO program, we have also been successful in getting interest from LumiLEDs in the InGaP/GaP work seeded in this program. With the interest from LumiLEDs, MIT was able to start an NSF GOALI program on ETS LEDs. Thus, the ARO funding has further been enhanced with NSF funds, as well as creating a pathway for potential commercialization of ARO-funded research.